

August 1991

Features

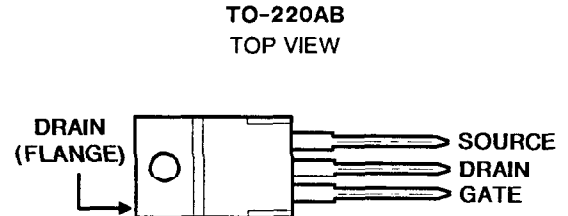
- 8.0A and 9.0A, 150V - 200V
- $r_{DS(on)} = 0.4\Omega$ and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRF630, IRF631, IRF632, and IRF633 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF630R, IRF631R, IRF632R and IRF633R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

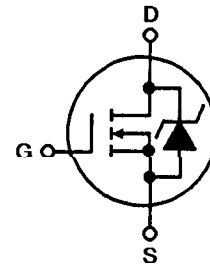
The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRF630 IRF630R	IRF631 IRF631R	IRF632 IRF632R	IRF633 IRF633R	UNITS
Drain-Source Voltage (1)	V_{DS} 200	150	200	150	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 200	150	200	150	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 9.0	9.0	8.0	8.0	A
$T_C = +100^\circ\text{C}$	I_D 6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3)	I_{DM} 36	36	32	32	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 36	36	32	32	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (4)	E_{AS}^* 150	150	150	150	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
 3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
 4. $V_{DD} = 20\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 0.07\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 9\text{A}$. See Figure 15.
- *R Suffix Types Only

IRF630, IRF631, IRF632, IRF633 IRF630R, IRF631R, IRF632R, IRF633R

Electrical Characteristics $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF630/632, IRF630R/632R IRF631/633, IRF631R/633R	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	200	-	-	V
			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	250	μA
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_J = +125^\circ\text{C}$	-	-	1000	μA
On-State Drain Current (Note 2) IRF630/631, IRF630R/631R IRF632/633, IRF632R/633R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON) \text{ Max}}, V_{GS} = 10V$	9.0	-	-	A
			8.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF630/631, IRF630R/631R IRF632/633, IRF632R/633R	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 5.0A$	-	0.25	0.4	Ω
			-	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times R_{DS(ON) \text{ Max}}, I_D = 5.0A$	3.0	4.8	-	S(V)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$	-	600	-	pF
Output Capacitance	C_{OSS}	See Figure 10	-	250	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	80	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 90V, I_D = 9.0A, R_G = 9.1\Omega$	-	-	30	ns
Rise Time	t_r	See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	50	ns
Fall Time	t_f		-	-	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V, I_D = 9.0A, V_{DS} = 0.8V \text{ Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)}$	-	19	30	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	9.0	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	$^\circ\text{C/W}$
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	$^\circ\text{C/W}$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	9.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	36	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^\circ\text{C}, I_S = 9.0A, V_{GS} = 0V$	-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = +150^\circ\text{C}, I_F = 9.0A, dI_F/dt = 100A/\mu s$	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +150^\circ\text{C}, I_F = 9.0A, dI_F/dt = 100A/\mu s$	-	3.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$

2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. $V_{DD} = 20V$, Start $T_J = +25^\circ\text{C}$, $L = 3.37\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 9A$ (See Figure 15)

IRF630, IRF631, IRF632, IRF633 IRF630R, IRF631R, IRF632R, IRF633R

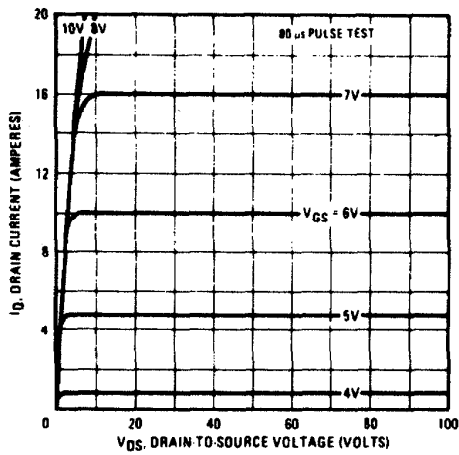


Fig. 1 - Typical Output Characteristics

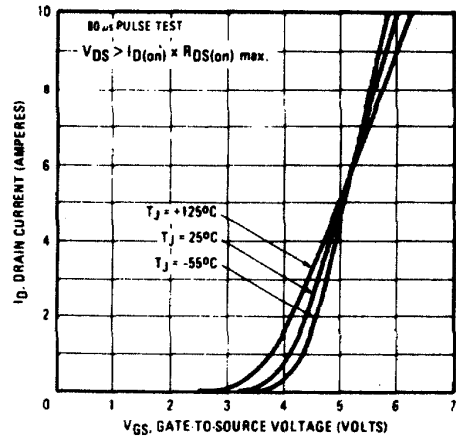


Fig. 2 - Typical Transfer Characteristics

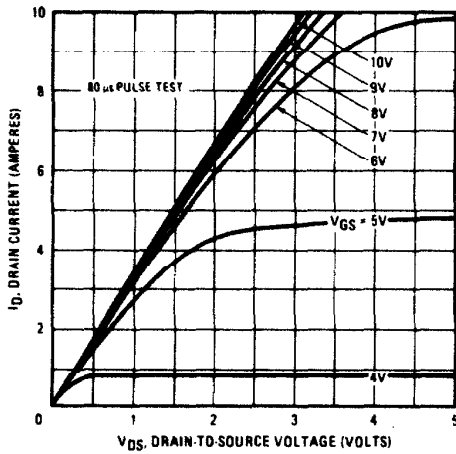


Fig. 3 - Typical Saturation Characteristics

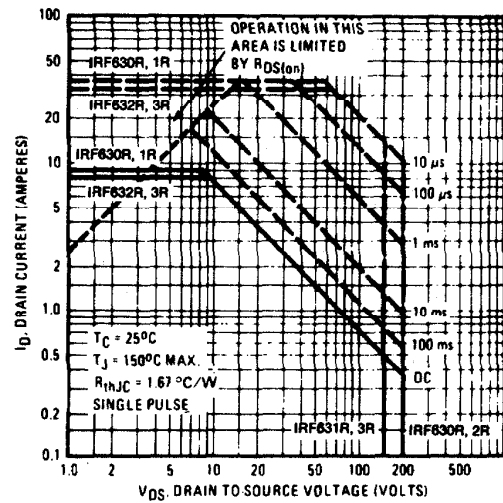


Fig. 4 - Maximum Safe Operating Area

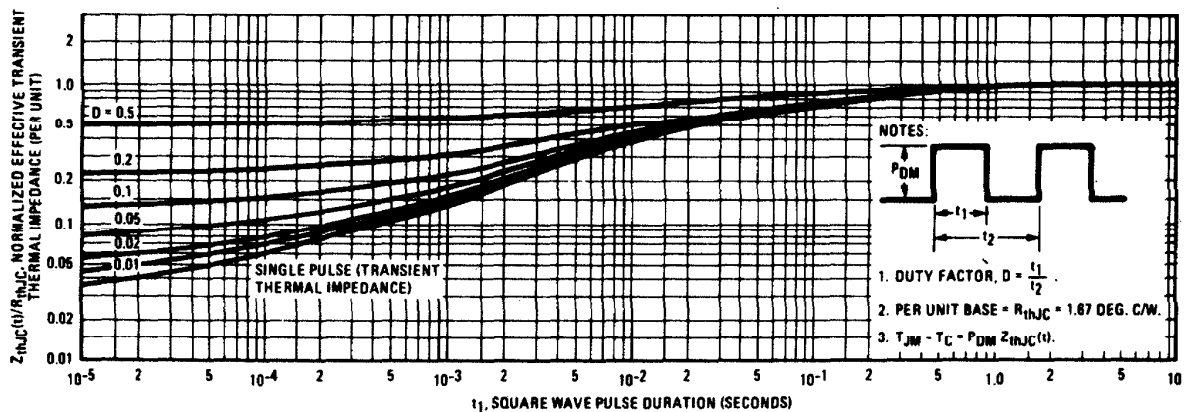


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

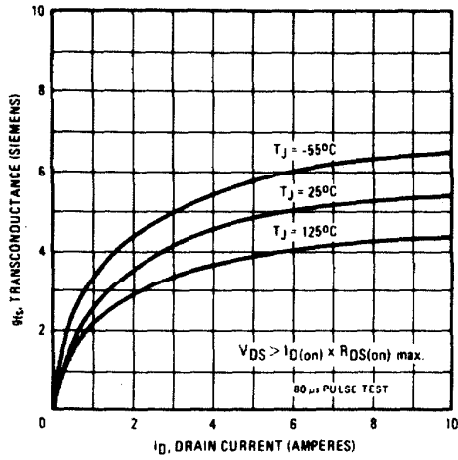


Fig. 6 – Typical Transconductance Vs. Drain Current

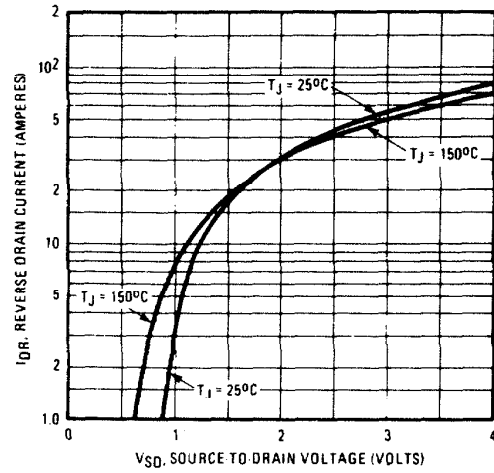


Fig. 7 – Typical Source-Drain Diode Forward Voltage

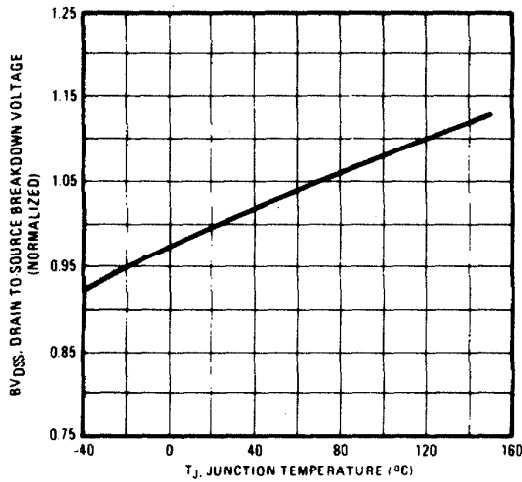


Fig. 8 – Breakdown Voltage Vs. Temperature

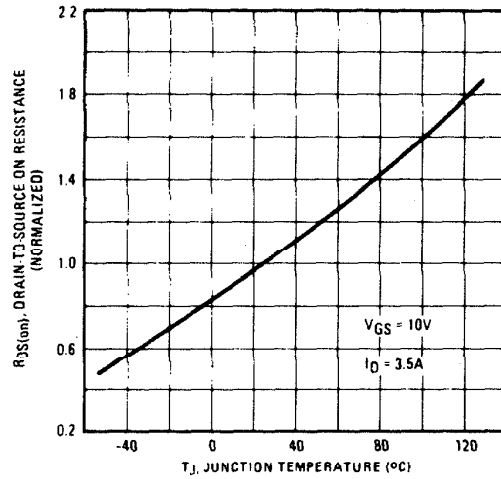


Fig. 9 – Normalized On-Resistance Vs. Temperature

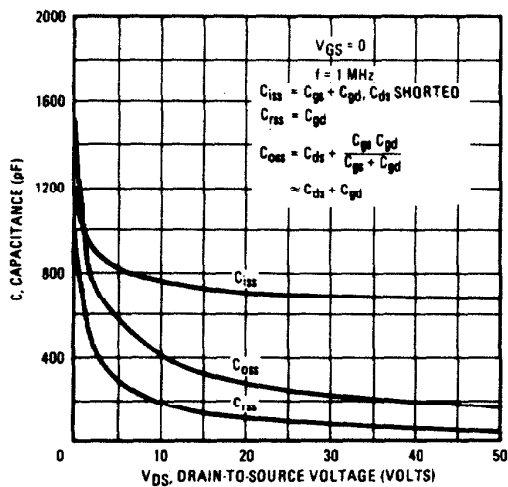


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

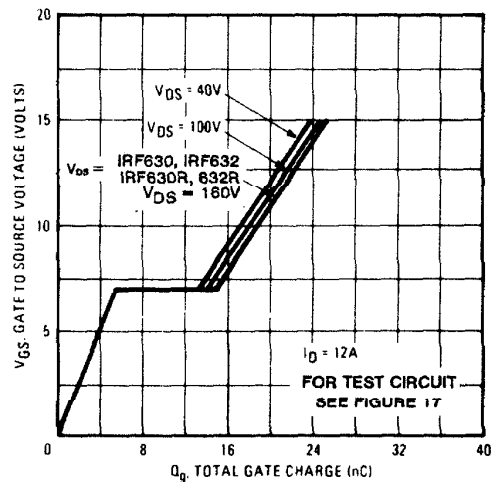


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

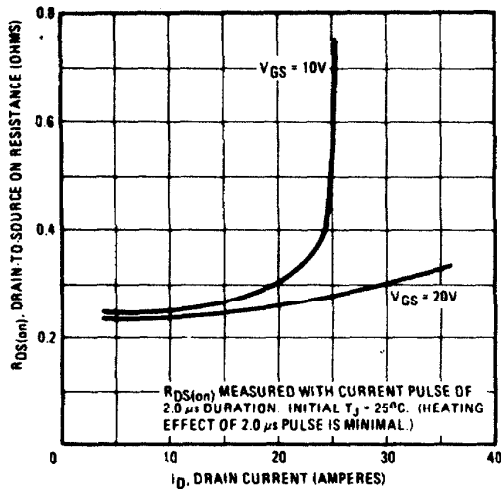


Fig. 12 — Typical On-Resistance Vs. Drain Current

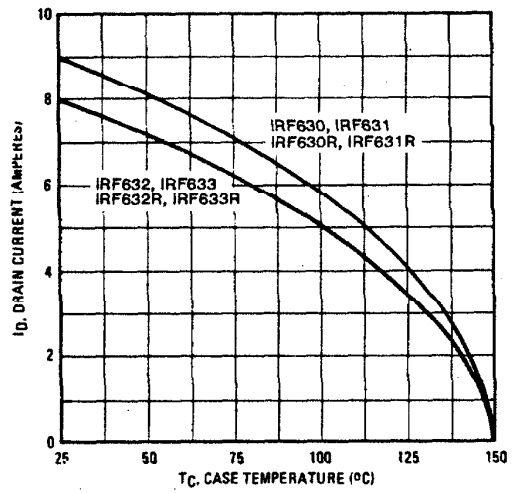


Fig. 13 — Maximum Drain Current Vs. Case Temperature

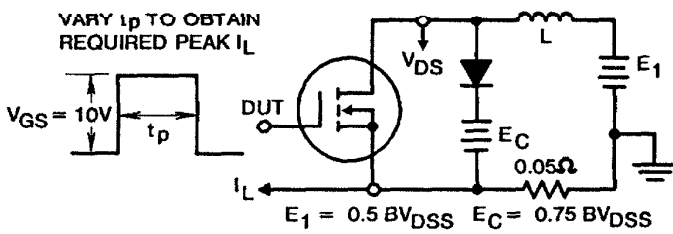


Fig. 14a — Clamped Inductive Test Circuit

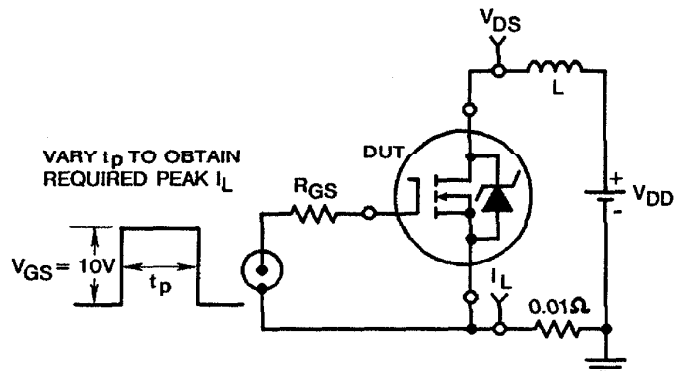


Fig. 15a — Unclamped Energy Test Circuit

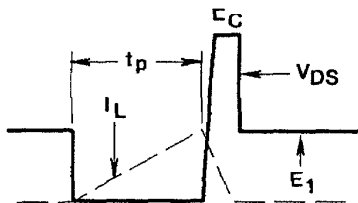


Fig. 14b — Clamped Inductive Waveforms

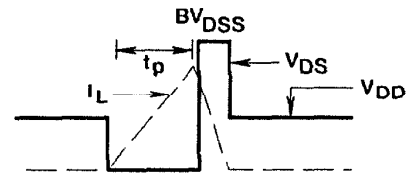


Fig. 15b — Unclamped Energy Waveforms

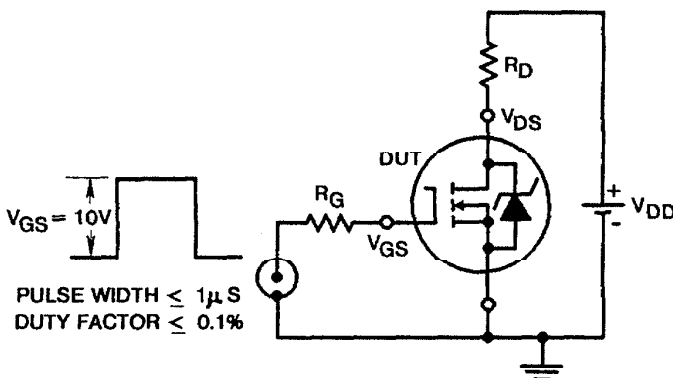


Fig. 16 — Switching Time Test Circuit

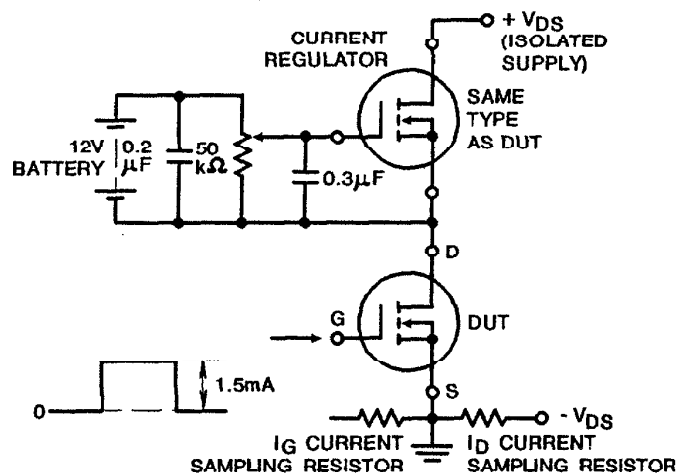


Fig. 17 — Gate Charge Test Circuit