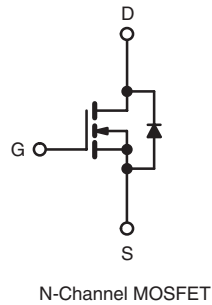
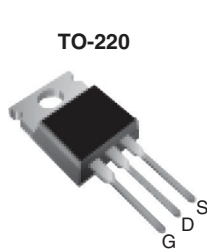


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	60 V	
R _{DS(on)} (Ω)	V _{GS} = 5.0 V	0.028
Q _g (Max.) (nC)	66	
Q _{gs} (nC)	12	
Q _{gd} (nC)	43	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- R_{DS(on)} Specified at V_{GS} = 4 V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRLZ44PbF
	SiHLZ44-E3
SnPb	IRLZ44
	SiHLZ44



ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Gate-Source Voltage	V _{GS}		± 10	V
Continuous Drain Current ^a	V _{GS} at 5.0 V	I _D	T _C = 25 °C	50
Continuous Drain Current			T _C = 100 °C	36
Pulsed Drain Current ^a			I _{DM}	200
Linear Derating Factor			1.0	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}		400	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	150
Peak Diode Recovery dV/dt ^c	dV/dt		4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}		- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s		300	
Mounting Torque	6-32 or M3 screw		10	
			1.1	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 179 μH, R_G = 25 Ω I_{AS} = 51 A (see fig. 12).
- I_{SD} ≤ 51 A, dV/dt ≤ 250 A/s, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.
- Current limited by the package, (die current = 51 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.070	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = 10\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$ $I_D = 31\text{ A}^b$	-	-	0.028	Ω
		$V_{GS} = 4.0\text{ V}$ $I_D = 25\text{ A}^b$	-	-	0.039	
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 31\text{ A}^b$	23	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	3300	-	pF
Output Capacitance	C_{oss}		-	1200	-	
Reverse Transfer Capacitance	C_{rss}		-	200	-	
Total Gate Charge	Q_g	$V_{GS} = 5.0\text{ V}$ $I_D = 51\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	66	nC
Gate-Source Charge	Q_{gs}		-	-	12	
Gate-Drain Charge	Q_{gd}		-	-	43	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 51\text{ A}$, $R_G = 4.6\text{ }\Omega$, $R_D = 0.56\text{ }\Omega$, see fig. 10 ^b	-	17	-	ns
Rise Time	t_r		-	230	-	
Turn-Off Delay Time	$t_{d(off)}$		-	42	-	
Fall Time	t_f		-	110	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	50 ^c	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	200	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 51\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 51\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	130	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.84	1.3	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Current limited by the package, (die current = 51 A).

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

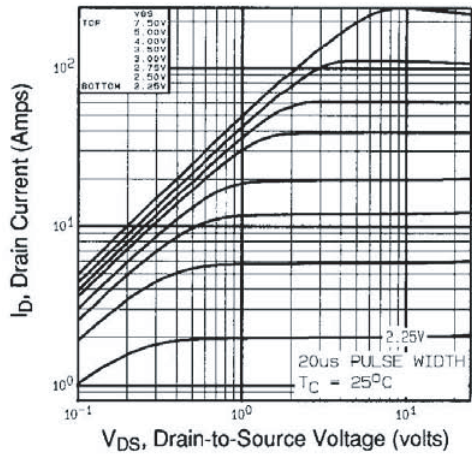


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

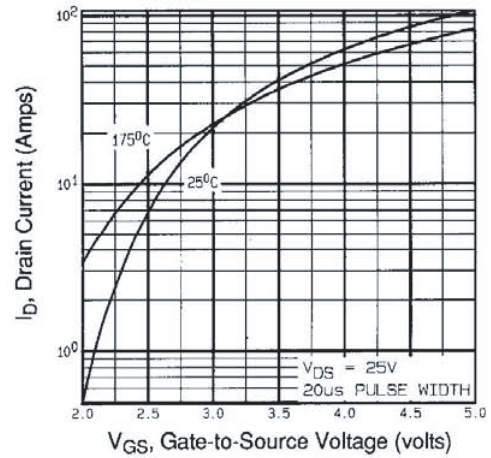


Fig. 3 - Typical Transfer Characteristics

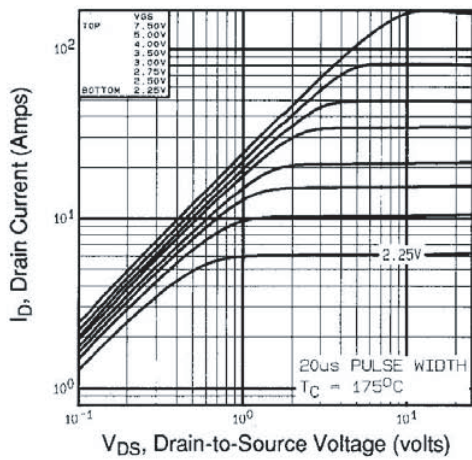


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

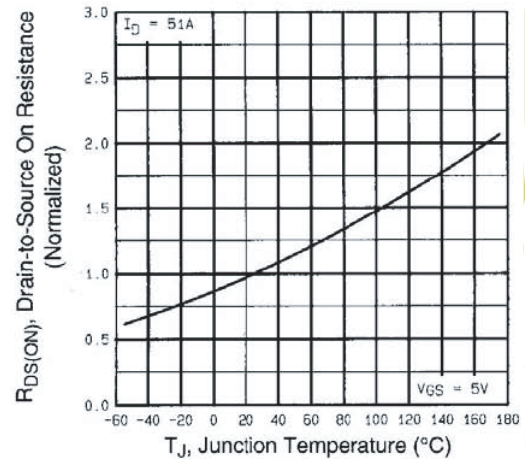


Fig. 4 - Normalized On-Resistance vs. Temperature

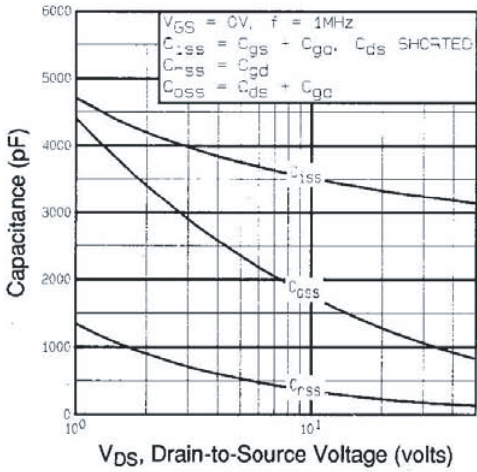


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

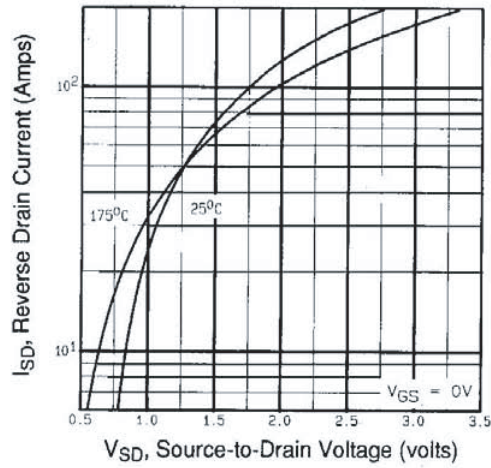


Fig. 7 - Typical Source-Drain Diode Forward Voltage

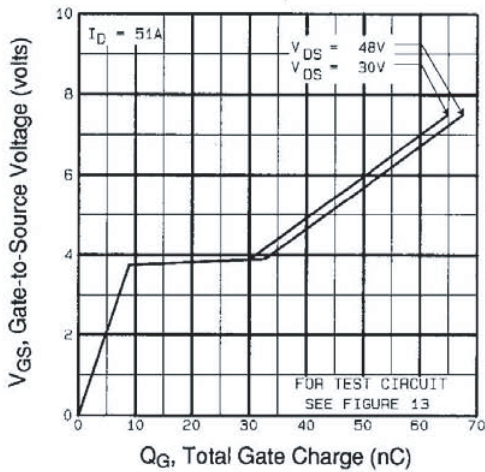


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

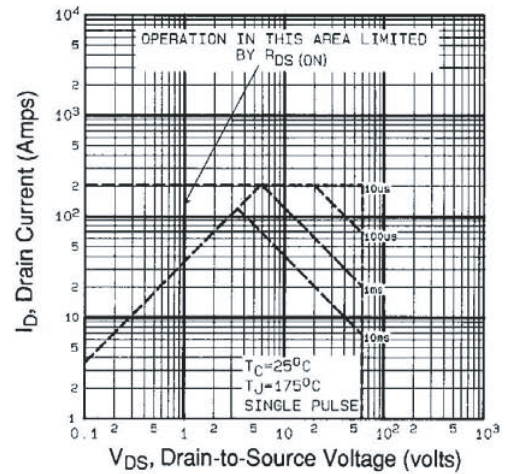


Fig. 8 - Maximum Safe Operating Area

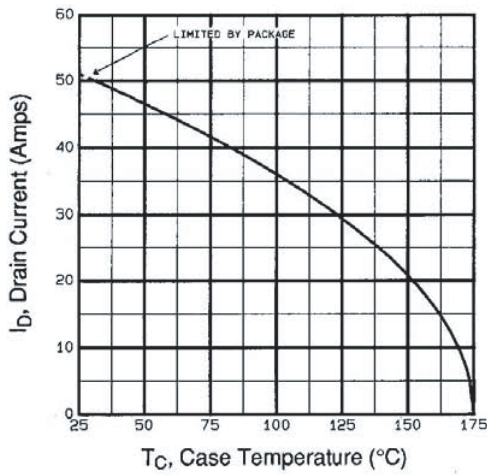


Fig. 9 - Maximum Drain Current vs. Case Temperature

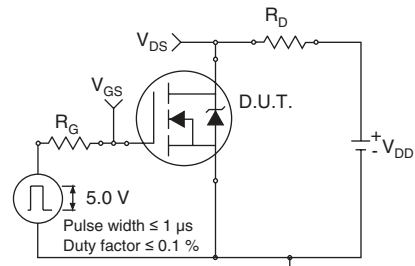


Fig. 10a - Switching Time Test Circuit

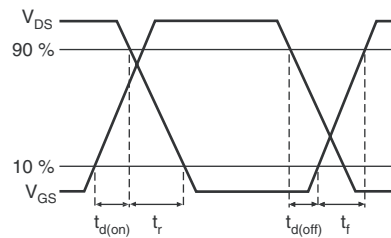


Fig. 10b - Switching Time Waveforms

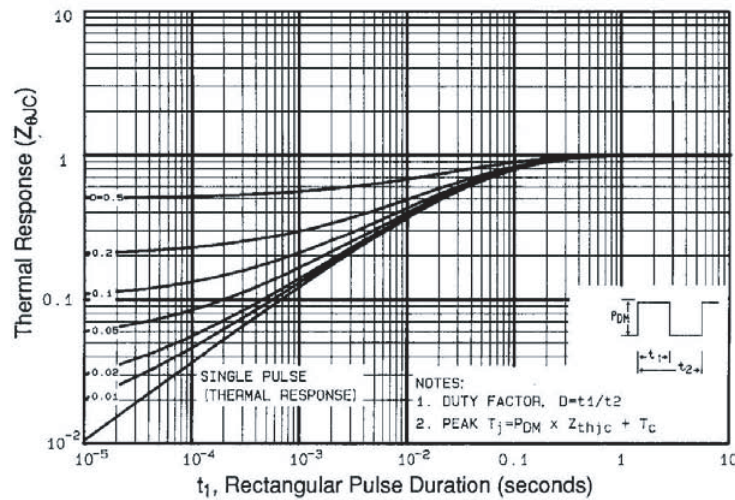


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

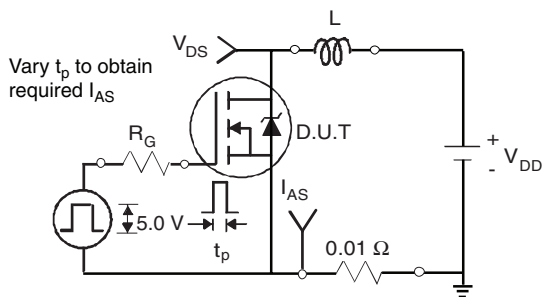


Fig. 12a - Unclamped Inductive Test Circuit

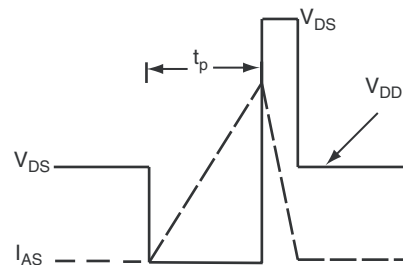


Fig. 12b - Unclamped Inductive Waveforms

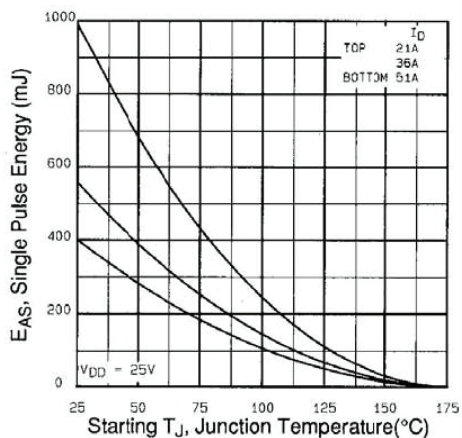


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

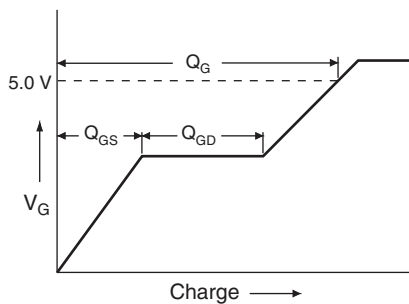


Fig. 13a - Basic Gate Charge Waveform

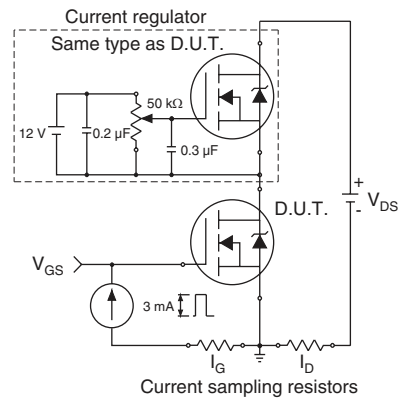
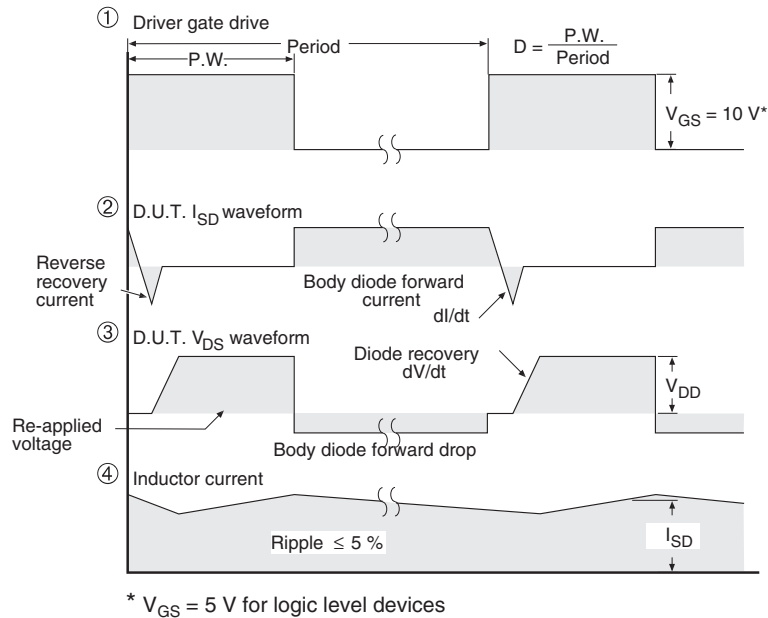
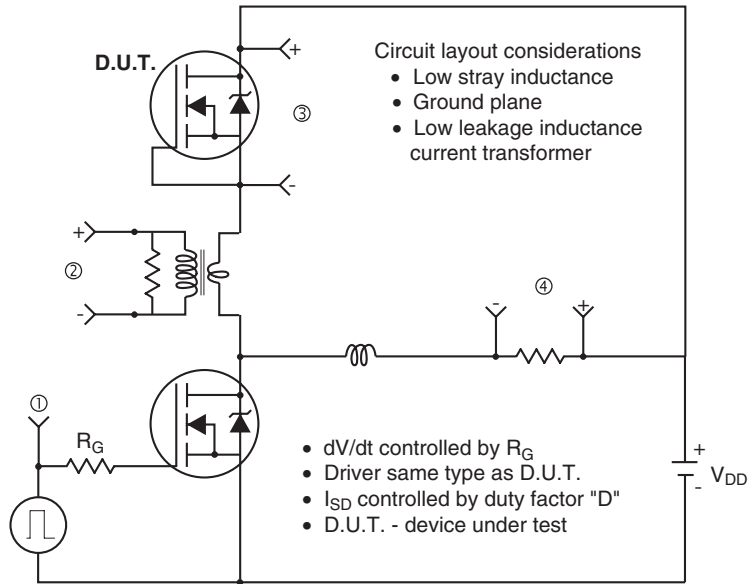


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Fig. 14 - For N-Channel

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