

FDMC8651

N-Channel Power Trench® MOSFET 30 V, 20 A, 6.1 mΩ

Features

- Max $r_{DS(on)}$ = 6.1 mΩ at $V_{GS} = 4.5$ V, $I_D = 15$ A
- Max $r_{DS(on)}$ = 9.3 mΩ at $V_{GS} = 2.5$ V, $I_D = 12$ A
- Low Profile - 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

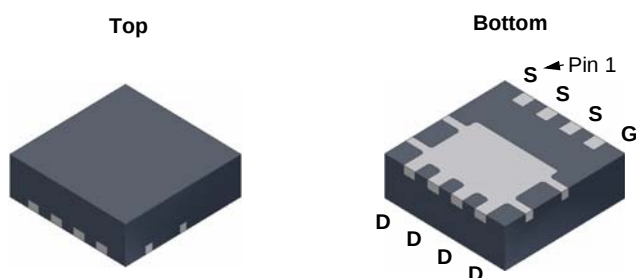


General Description

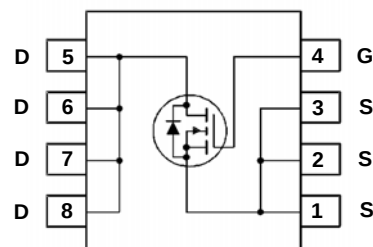
This device has been designed specifically to improve the efficiency of DC/DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low $r_{DS(on)}$ has been maintained to provide a sub logic-level device.

Applications

- Synchronous rectifier
- 3.3 V input synchronous buck switch



Power 33



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	20	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	64	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	15	
	-Pulsed	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	128	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	41	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8651	FDMC8651	Power 33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		27.5		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	0.8	1.1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-4.4		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 15\text{ A}$		4.3	6.1	m Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 12\text{ A}$		6.2	9.3	
		$V_{GS} = 4.5\text{ V}$, $I_D = 15\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		6.3	9.0	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 15\text{ A}$		91		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2530	3365	pF
C_{oss}	Output Capacitance			865	1150	pF
C_{rss}	Reverse Transfer Capacitance			140	205	pF
R_g	Gate Resistance			0.8		Ω

Switching Characteristics

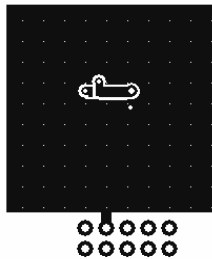
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		18	31	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			35	56	ns
t_f	Fall Time			6	12	ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5 V	$V_{DD} = 15\text{ V}$, $I_D = 15\text{ A}$		19.4	27.2	nC
Q_{gs}	Total Gate Charge			4.8		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.2		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 15\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = 1.7\text{ A}$ (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		35	55	ns
Q_{rr}	Reverse Recovery Charge			17	30	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 $^{\circ}\text{C}/\text{W}$ when mounted on a
1 in² pad of 2 oz copper



b. 125 $^{\circ}\text{C}/\text{W}$ when mounted on
a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^{\circ}\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 16\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

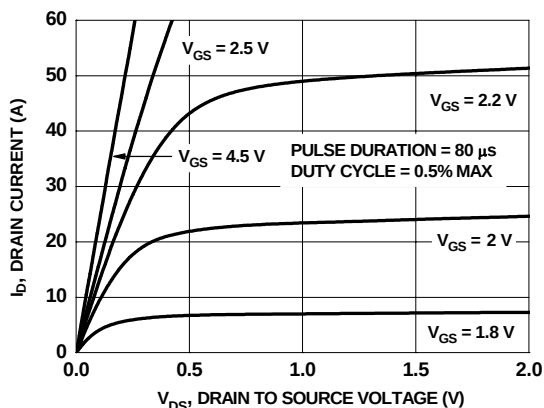


Figure 1. On-Region Characteristics

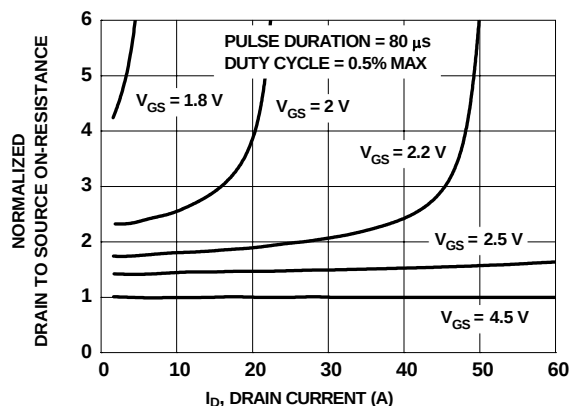


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

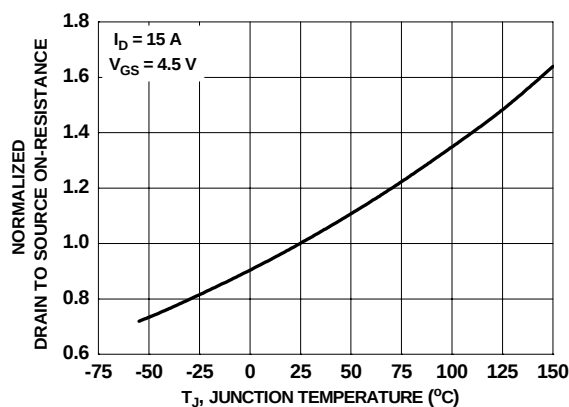


Figure 3. Normalized On-Resistance vs Junction Temperature

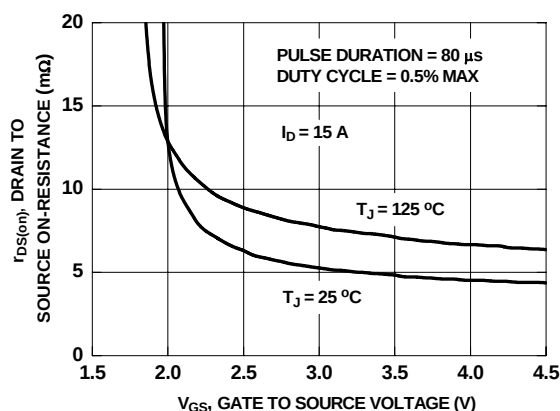


Figure 4. On-Resistance vs Gate to Source Voltage

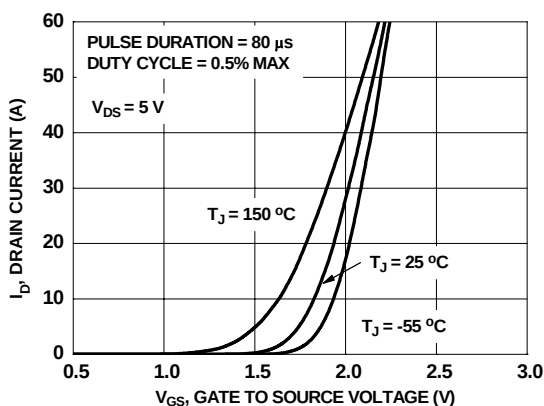


Figure 5. Transfer Characteristics

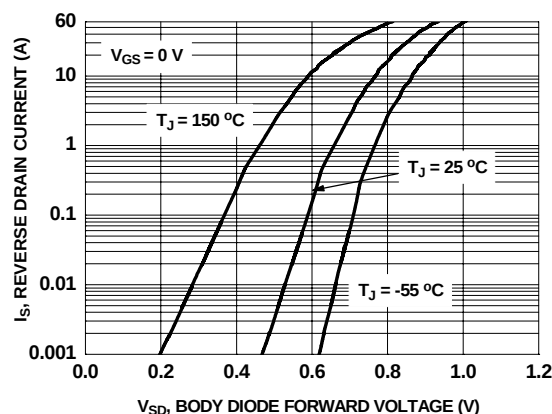


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

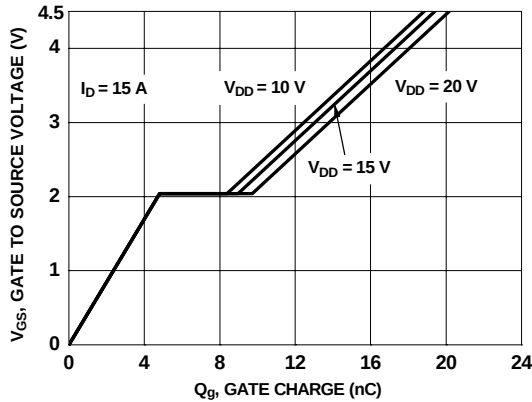


Figure 7. Gate Charge Characteristics

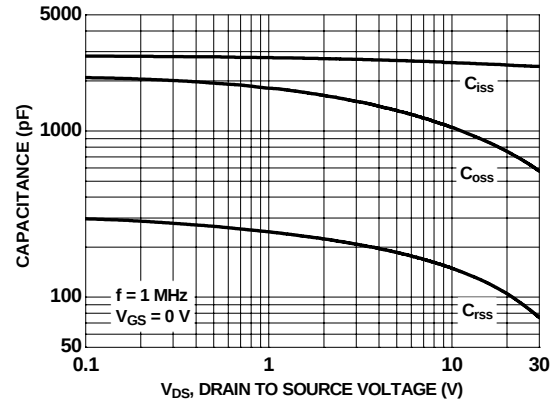


Figure 8. Capacitance vs Drain to Source Voltage

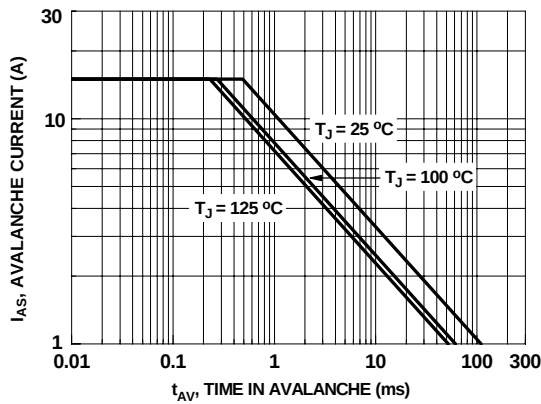


Figure 9. Unclamped Inductive Switching Capability

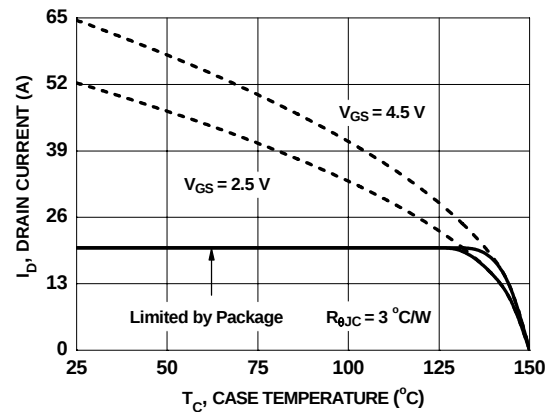


Figure 10. Maximum Continuous Drain Current vs Case Temperature

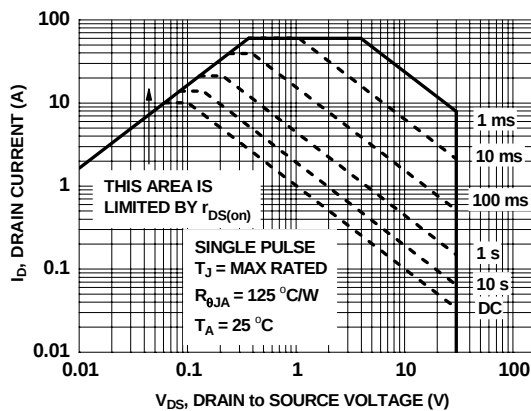


Figure 11. Forward Bias Safe Operating Area

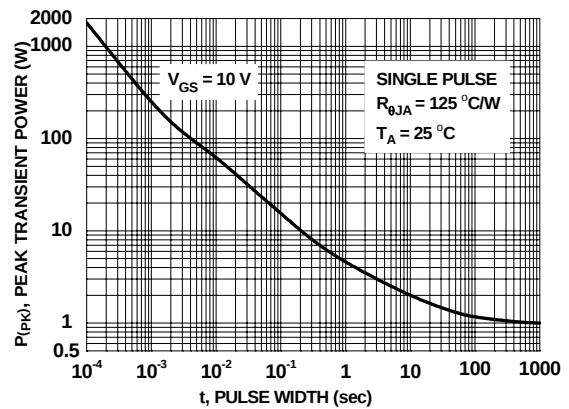
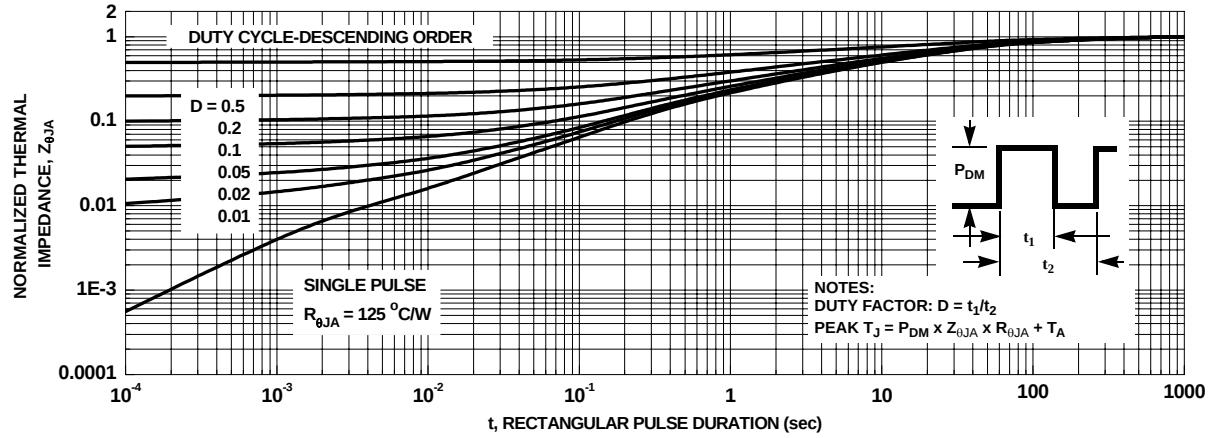
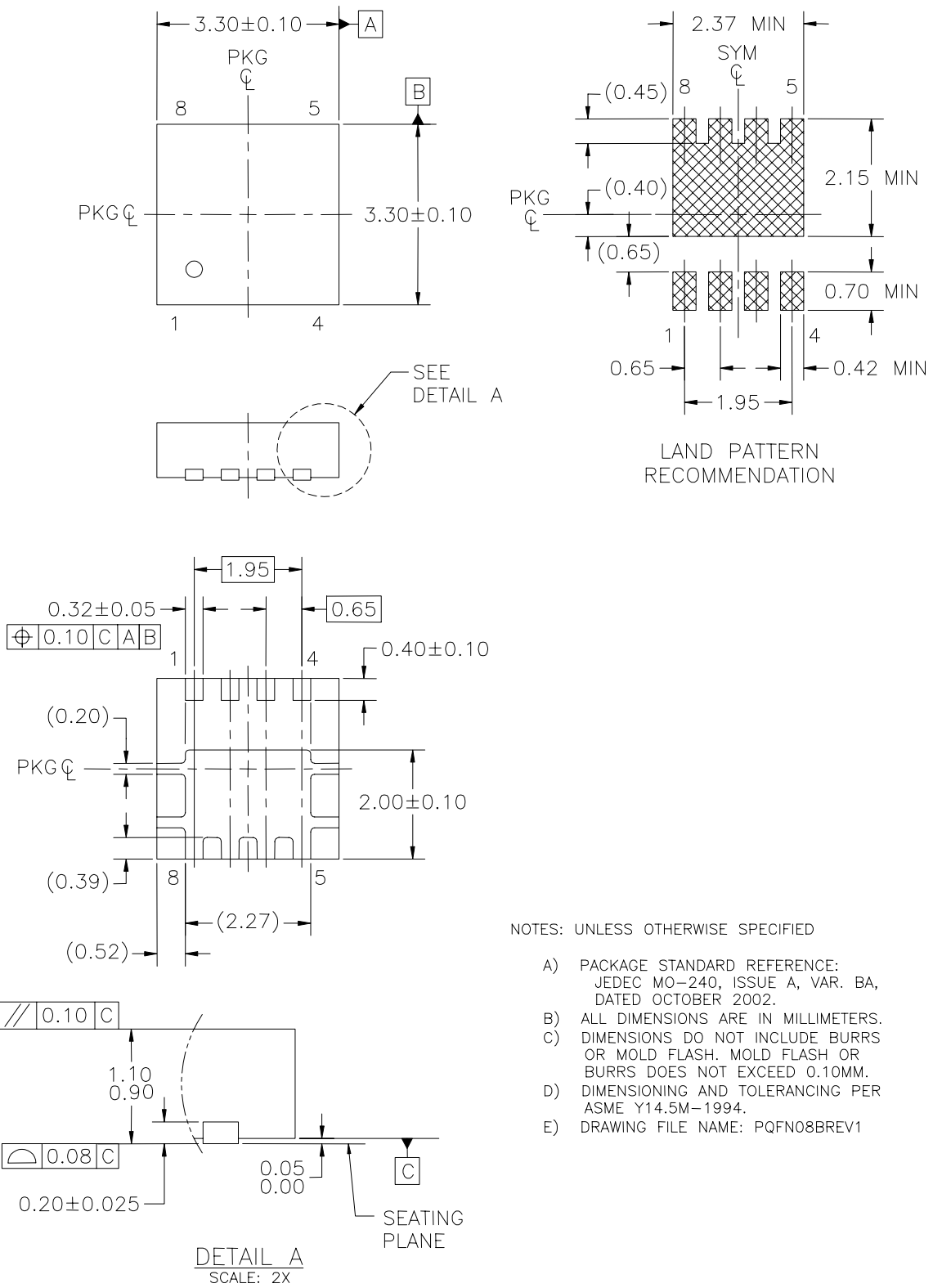


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



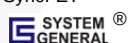
Dimensional Outline and Pad Layout



PQFN08BREV1

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