

Features

- Very high speed: 45
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V–3.60 V
- Pin compatible with CY62137CV/CV25/CV30/CV33, CY62137V, and CY62137EV30
- Ultra low standby power
 - Typical standby current: 1 µA
 - Maximum standby current: 5 µA (Industrial)
- Ultra low active power
 - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Byte power down feature
- Available in Pb free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II package

Functional Description

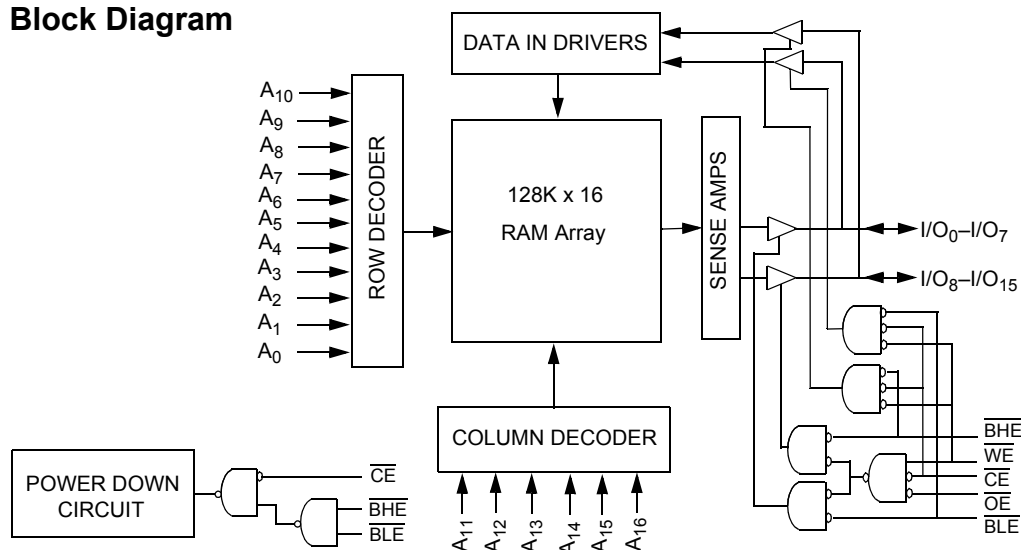
The CY62137FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state in the following conditions when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both the Byte High Enable and the Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during an active write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW, while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



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Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1MHz		f = f _{max}							
		Min	Typ ^[1]	Max		Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62137FV30LL	Industrial	2.2 V	3.0 V	3.6 V	45	1.6	2.5	13	18	1	5

Pin Configuration

Figure 1. 48-ball VFBGA pinout ^[2, 3]

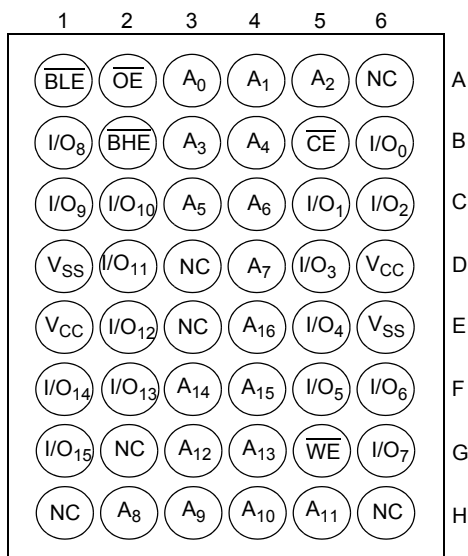
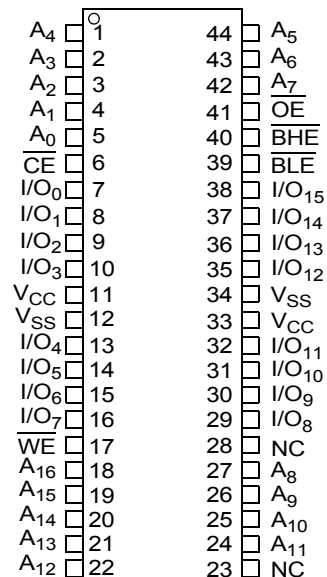


Figure 2. 44-pin TSOP II pinout ^[2]



Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage to ground potential [4, 5] -0.3 V to 3.9 V

DC voltage applied
to outputs in High Z state [4, 5] -0.3 V to 3.9 V

DC input voltage [4, 5] -0.3 V to 3.9 V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, method 3015) > 2001 V

Latch up current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} [6]
CY62137FV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial)			Unit
			Min	Typ [7]	Max	
V _{OH}	Output high voltage	2.2 ≤ V _{CC} ≤ 2.7 I _{OH} = -0.1 mA	2.0	—	—	V
		2.7 ≤ V _{CC} ≤ 3.6 I _{OH} = -1.0 mA	2.4	—	—	V
V _{OL}	Output low voltage	2.2 ≤ V _{CC} ≤ 2.7 I _{OL} = 0.1 mA	—	—	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6 I _{OL} = 2.1 mA	—	—	0.4	V
V _{IH}	Input high voltage	2.2 ≤ V _{CC} ≤ 2.7	1.8	—	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input low voltage	2.2 ≤ V _{CC} ≤ 2.7	-0.3	—	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6	-0.3	—	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	—	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled	-1	—	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC} V _{CC} = V _{CC(max)} f = 1 MHz I _{OUT} = 0 mA CMOS levels	—	13	18	mA
			—	1.6	2.5	
I _{SB1} [8]	Automatic power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V, or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE and WE), V _{CC} = V _{CC(max)}	—	1	5	μA
I _{SB2} [8]	Automatic power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)}	—	1	5	μA

Notes

4. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.

5. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.

6. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C

8. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

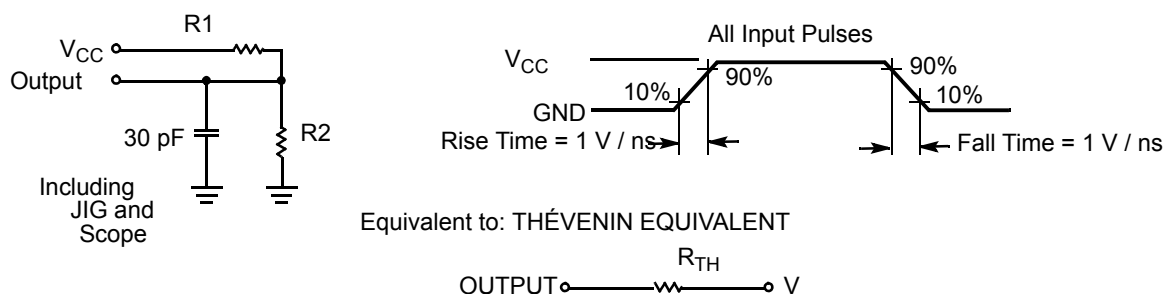
Parameter ^[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, two layer printed circuit board	75	77	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		10	13	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Notes

9. Tested initially and after any design or process changes that may affect these parameters.

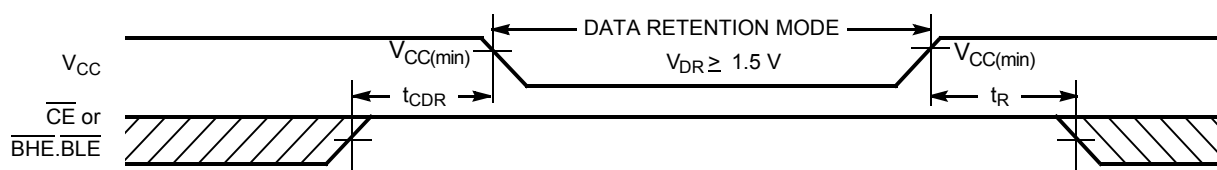
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
$I_{CCDR}^{[11]}$	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2\text{ V}$ $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	4	μA
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[13]}$	Operation recovery time	CY62137FV30LL-45	45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform ^[14]



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu\text{s}$ or stable at $V_{CC(min)} \geq 100\ \mu\text{s}$.
14. $\overline{BHE.BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter ^[15, 16]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45	–	ns
t _{AA}	Address to data valid	–	45	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t _{LZOE}	$\overline{OE}$ LOW to low Z ^[17]	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to high Z ^[17, 18]	–	18	ns
t _{LZCE}	$\overline{CE}$ LOW to low Z ^[17]	10	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to high Z ^[17, 18]	–	18	ns
t _{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[17, 19]	5	–	ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[17, 18]	–	18	ns
Write Cycle ^[20, 21]				
t _{WC}	Write cycle time	45	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t _{AW}	Address setup to write end	35	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	35	–	ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to high Z ^[17, 18]	–	18	ns
t _{LZWE}	$\overline{WE}$ HIGH to low Z ^[17]	10	–	ns

Notes

15. Test conditions for all parameters, other than tristate parameters, assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [AC Test Loads and Waveforms on page 5](#).
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for WRITE Cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle 1: Address Transition Controlled [22, 23]

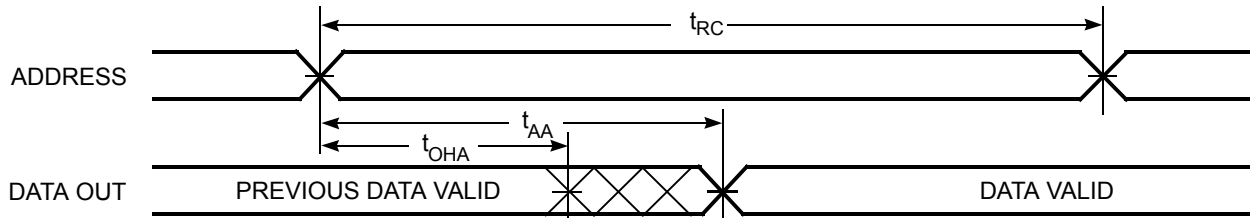
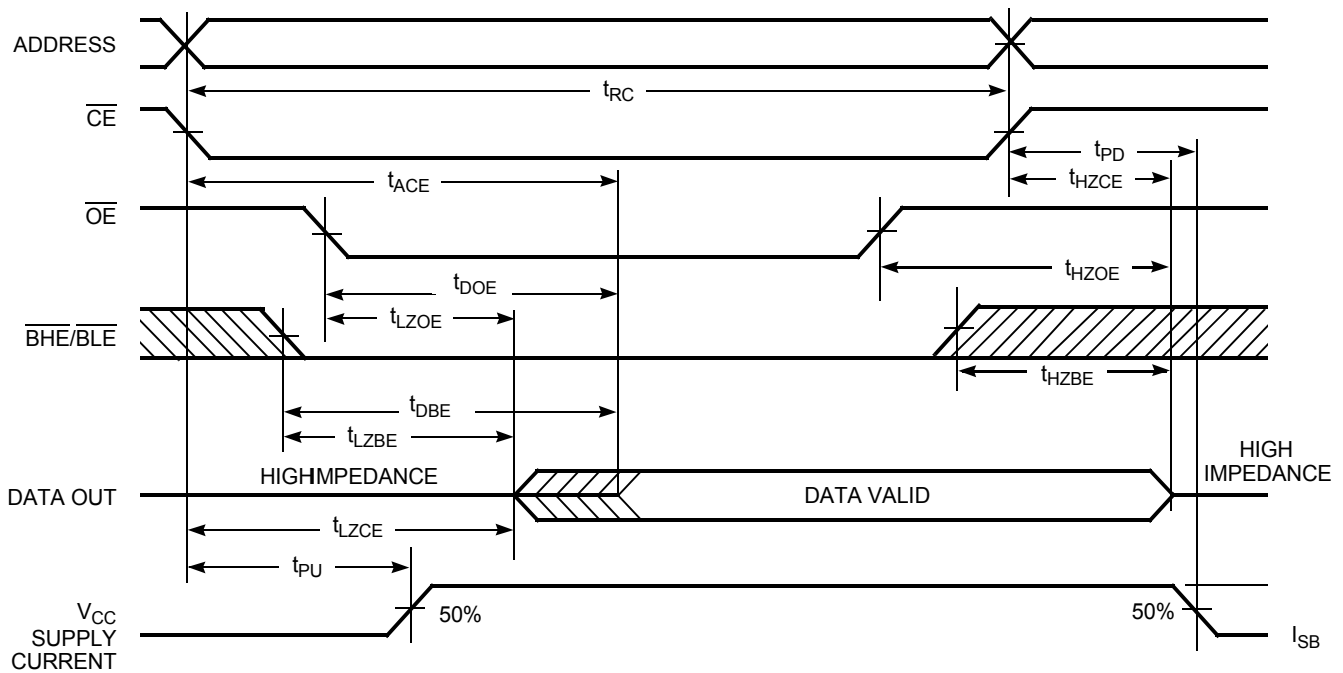


Figure 6. Read Cycle 2: $\overline{\text{OE}}$ Controlled [23, 24]



Notes

22. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$.

23. $\overline{\text{WE}}$ is HIGH for read cycle.

24. Address valid before or similar to $\overline{\text{CE}}$ and $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle 1: $\overline{WE}$ Controlled [25, 26, 27]

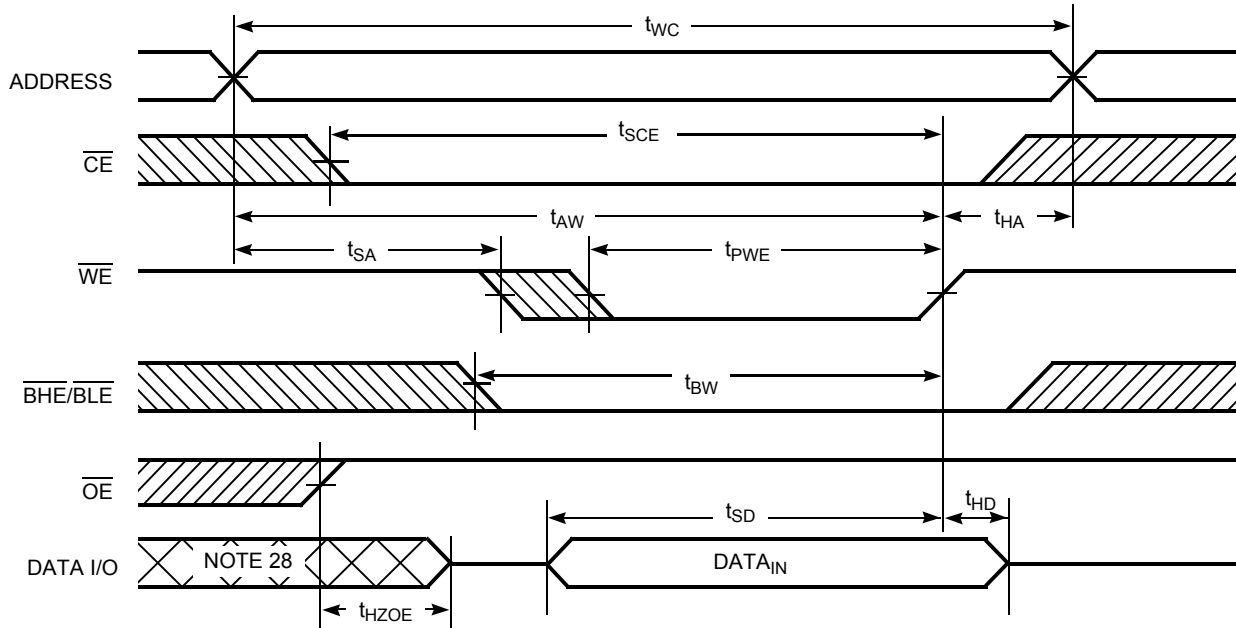
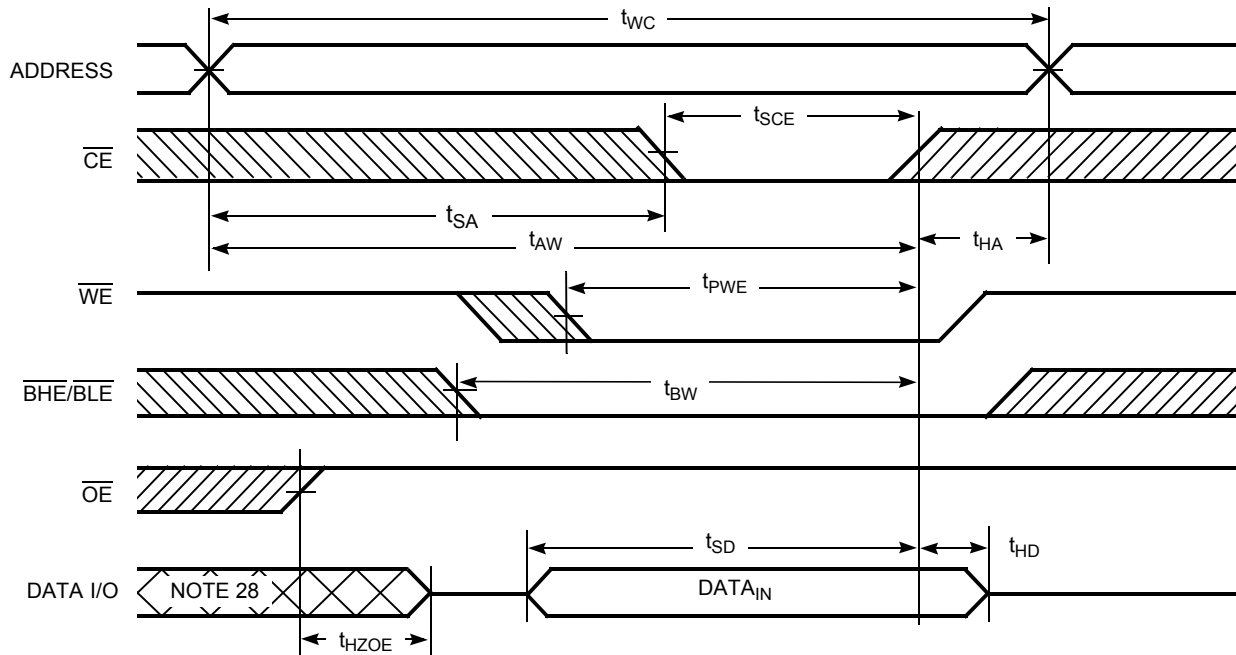


Figure 8. Write Cycle 2: $\overline{CE}$ Controlled [25, 26, 27]



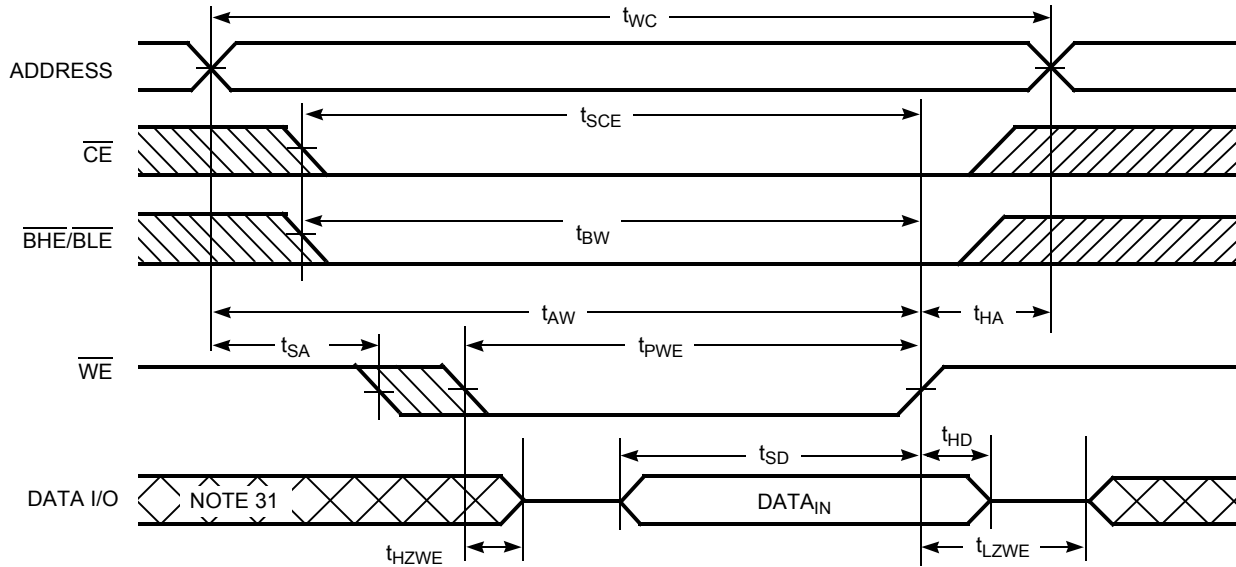
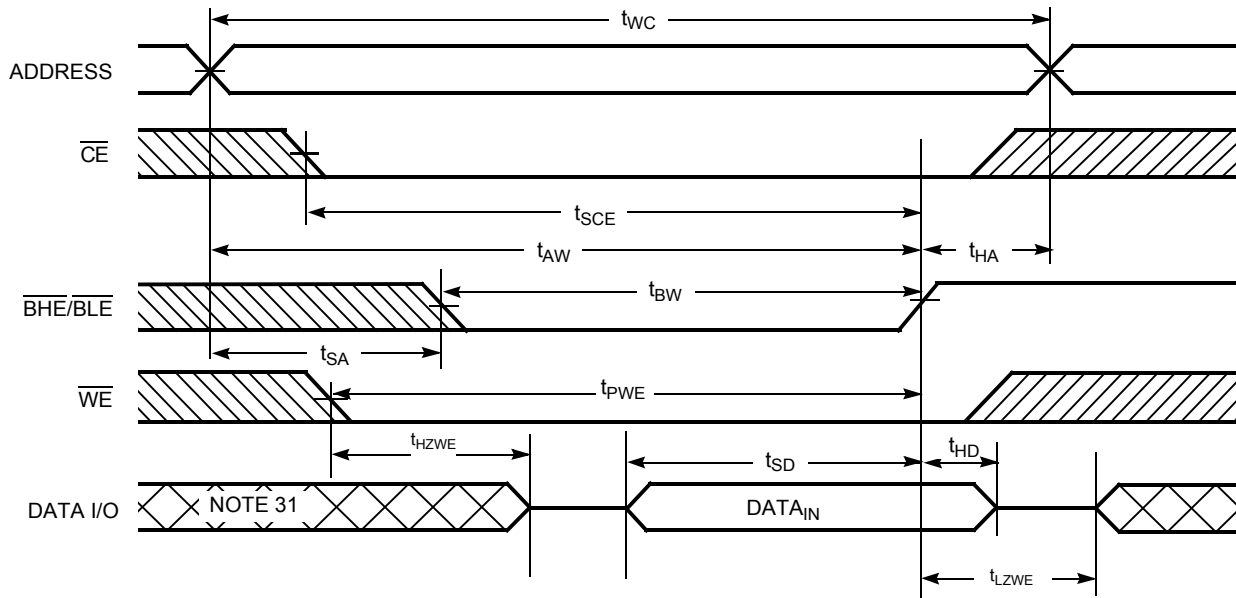
Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Figure 9. Write Cycle 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [29, 30]

Figure 10. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [29]

Notes

29. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

30. The minimum write cycle pulse width for WRITE Cycle 1 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

CE	WE	OE	BHE	BLE	Inputs or Outputs	Mode	Power
H	X	X	X ^[32]	X ^[32]	High Z	Deselect or power-down	Standby (I _{SB})
X ^[32]	X	X	H	H	High Z	Deselect or power-down	Standby (I _{SB})
L	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I _{CC})
L	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I _{CC})
L	H	H	L	L	High Z	Output disabled	Active (I _{CC})
L	H	H	H	L	High Z	Output disabled	Active (I _{CC})
L	H	H	L	H	High Z	Output disabled	Active (I _{CC})
L	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})

Note

32. The 'X' (Don't care) state for the Chip enable ($\overline{\text{CE}}$) and Byte enables ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137FV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62137FV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Temperature Grade: I = Industrial

Pb-free

Package Type: XX = BV or ZS
BV = 48-ball VFBGA
ZS = 44-pin TSOP II

Speed Grade: 45 ns

Low Power

Voltage Range: V30 = 3 V typical

Process Technology: F = 90 nm

Bus width: 7 = × 16

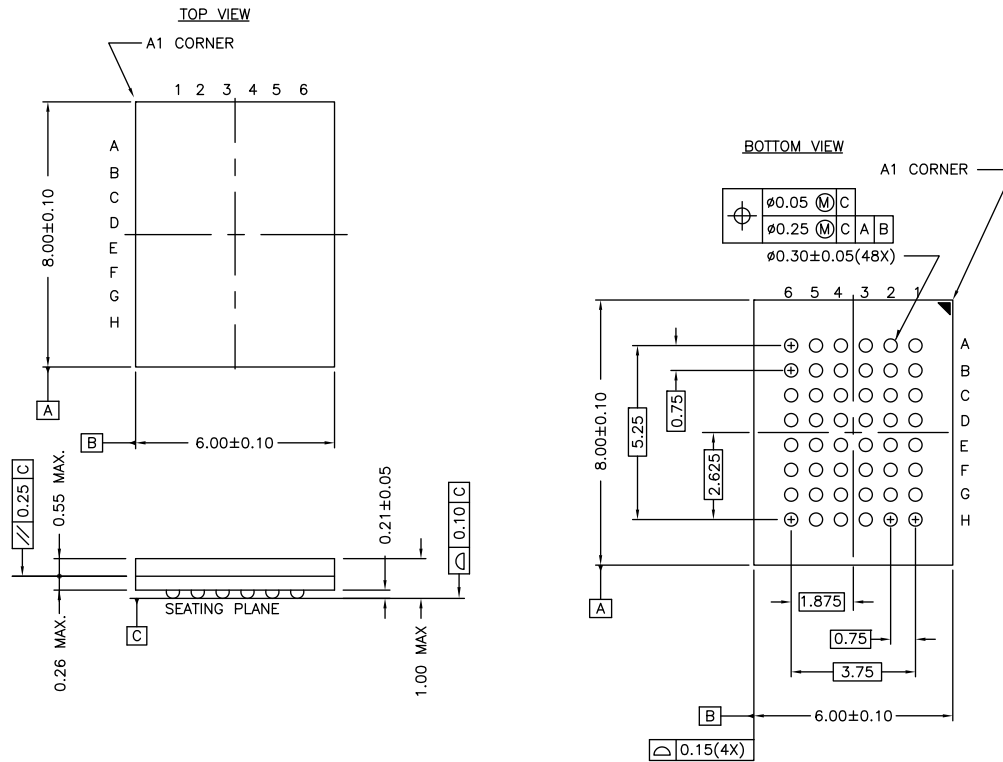
Density: 3 = 2-Mbit

Family Code: 621= MoBL SRAM family

Company ID: CY = Cypress

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

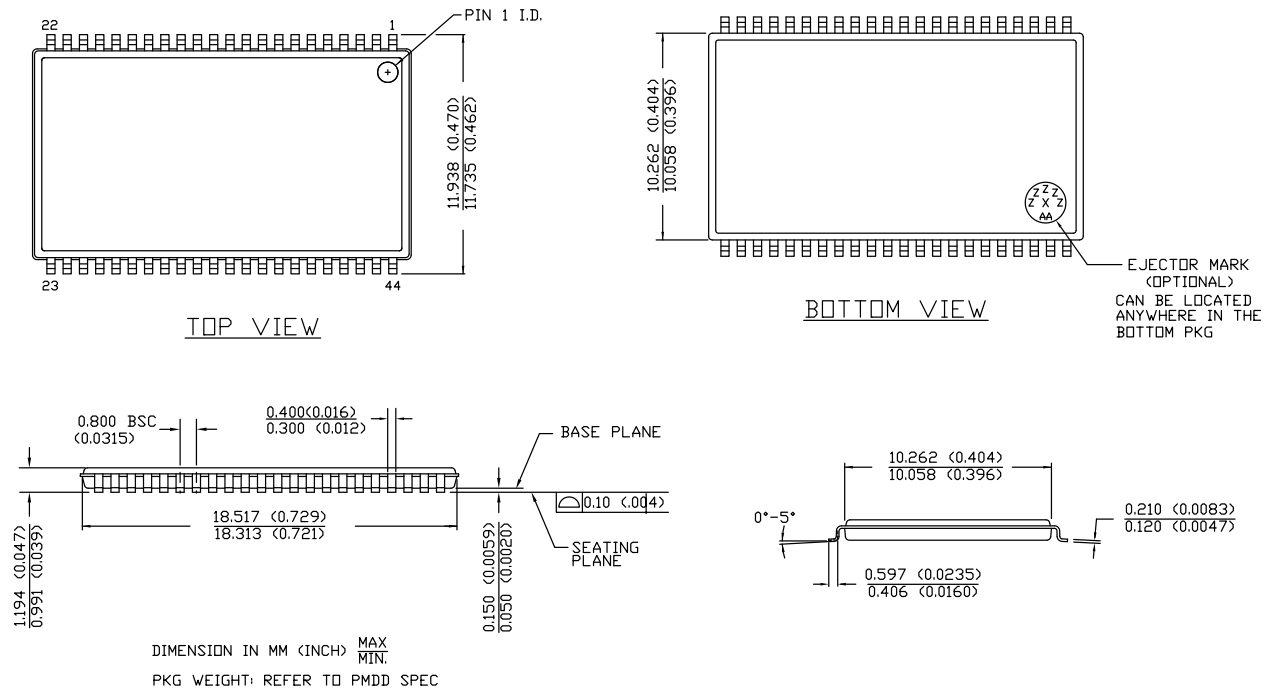


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62137FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-07141				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	449438	See ECN	NXR	New data sheet.
*A	464509	See ECN	NXR	Changed the $I_{SB2(typ)}$ value from 1.0 μA to 0.5 μA Changed the $I_{SB2(max)}$ value from 4 μA to 2.5 μA Changed the $I_{CC(typ)}$ value from 2 mA to 1.6 mA and $I_{CC(max)}$ value from 2.5 mA to 2.25 mA for $f = 1$ MHz test condition Changed the $I_{CC(typ)}$ value from 15 mA to 13 mA and $I_{CC(max)}$ value from 20 mA to 18 mA for $f = 1$ MHz test condition Changed the $I_{CCDR(typ)}$ value from 0.7 μA to 0.5 μA and $I_{CCDR(max)}$ value from 3 μA to 2.5 μA
*B	566724	See ECN	NXR	Changed status from preliminary to final Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition $f = 1$ MHz Changed the $I_{SB2(typ)}$ value from 0.5 μA to 1 μA Changed the $I_{SB2(max)}$ value from 2.5 μA to 5 μA Changed the $I_{CCDR(typ)}$ value from 0.5 μA to 1 μA and $I_{CCDR(max)}$ value from 2.5 μA to 4 μA
*C	869500	See ECN	VKN	Added Automotive-A and Automotive-E information Updated Ordering Information Table Added footnote 13 related to t_{ACE}
*D	901800	See ECN	VKN	Added footnote 9 related to I_{SB2} and I_{CCDR} Made footnote 14 applicable to AC parameters from t_{ACE}
*E	1371124	See ECN	VKN / AESA	Converted Automotive information from preliminary to final Changed I_{IX} min spec from -1 μA to -4 μA and I_{IX} max spec from +1 μA to +4 μA Changed I_{OZ} min spec from -1 μA to -4 μA and I_{OZ} max spec from +1 μA to +4 μA
*F	1875374	See ECN	VKN / AESA	Added -45BVI part in the Ordering Information table
*G	2943752	06/03/2010	VKN	Added Contents Added footnote related to Chip enable and Byte enables in Truth Table Updated Package Diagrams Updated links in Sales, Solutions, and Legal Information
*H	3055031	10/12/10	RAME	Converted all table notes into footnotes. Updated Electrical Characteristics . Changed $I_{SB1}/I_{SB2}/I_{CCDR}$ test conditions to reflect byte power down feature Updated Data Retention Characteristics . Updated Switching Characteristics . Updated Package Diagrams from 51-85150 *E to *F Added Acronyms and Units of Measure .
*I	3123998	01/03/2011	RAME	Separated Automotive and Industrial parts from datasheet Removed Automotive info
*J	3285093	06/16/2011	RAME	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated in new template.
*K	3841412	12/14/2012	YHB / TAVA	Updated Ordering Information (Updated part numbers). Updated Package Diagrams (spec 51-85150 (Changed revision from *F to *H), spec 51-85087 (Changed revision from *C to *E)).
*L	4102022	08/22/2013	VINI	Updated Switching Characteristics : Updated Note 16. Updated to new template.

Document History Page (continued)

Document Title: CY62137FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-07141				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*M	4268388	01/31/2014	VINI	No technical updates. Completing Sunset Review.
*N	4472487	08/13/2014	NILE	Updated Maximum Ratings : Referred Note 4 in “DC input voltage” parameter. Updated Switching Characteristics : Added Note 21 and referred the same note in “Write Cycle”. Updated Switching Waveforms : Added Note 30 and referred in Figure 9 .
*O	4576561	11/21/2014	NILE	Added related documentation hyperlink in page 1. Updated Figure 6 . Added shading to the BHE/BLE waveform. Completing Sunset Review.
*P	4613342	01/05/2015	VINI	Updated Maximum Ratings : Referred Notes 4, 5 in “Supply voltage to ground potential”.

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