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EVALUATING THE AD9653/AD9253/AD9633 ANALOG-TO-DIGITAL CONVERTERS

Preface

This user guide describes the AD9653, AD9253 and AD9633 evaluation boards, AD9653-125EBZ, AD9253-125EBZ and AD9633-125EBZ, which provide all of the support circuitry required to operate these parts in their various modes and configurations. The application software used to interface with the devices is also described.

The AD9653 AD9253 and AD9633 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/hsadcevalboard. For additional information or questions, send an email to highspeed.converters@analog.com.

Typical Measurement Setup

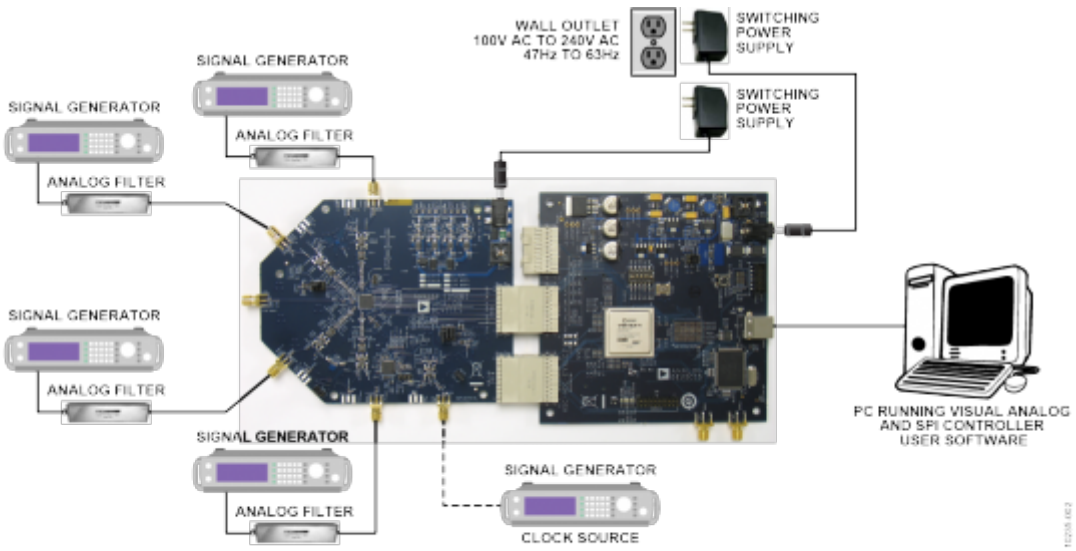


Figure 1. Evaluation Board Connection—AD9653-125EBZ, AD9253-125EBZ or AD9633-125EBZ (on Left) and HSC-ADC-EVALCZ (on Right)

Features

- Full featured evaluation board for the AD9653/AD9253/AD9633
- SPI interface for setup and control
- External, on-board oscillator, or AD9517 clocking option
- Balun/transformer or amplifier input drive option
- On-board LDO regulator needing a single external 6 V, 2 A dc supply
- VisualAnalog® and SPI controller software interfaces

Helpful Documents

- AD9653, AD9253 or AD9633 data sheet
- High speed ADC FIFO evaluation kit (HSC-ADC-EVALCZ)
- AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
- AN-878 Application Note, *High Speed ADC SPI Control Software*
- AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
- AN-835 Application Note, *Understanding ADC Testing and Evaluation*

Design and Integration Files

- Schematics, layout files, bill of materials

Equipment Needed

- Analog signal source and antialiasing filter
- Sample clock source (if not using the on-board oscillator)
- 2 switching power supplies (6.0 V, 2.5 A), CUI EPS060250UH-PHP-SZ provided
- PC running Windows®
- USB 2.0 port
- AD9653-125EBZ, AD9253-125EBZ or AD9633-125EBZ board
- HSC-ADC-EVALCZ FPGA-based data capture kit

Getting Started

This section provides quick start procedures for using the AD9653-125EBZ, AD9253-125EBZ or AD9633-125EBZ board. Both the default and optional settings are described.

Configuring the Board

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ that is supplied) to the AD9653-125EBZ, AD9253-125EBZ or AD9633-125EBZ.
3. Connect one 6 V, 2.5 A switching power supply (such as the supplied CUI EPS060250UH-PHP-SZ) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (J6) to the PC using a USB cable.
5. On the ADC evaluation board, confirm that the jumpers are installed as shown in Figure 2 and Table 1.
6. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the desired A and/or B channel(s). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices, Inc., uses TTE, Allen Avionics, and K&L band-pass filters.)

Evaluation Board Hardware

The evaluation board provides the support circuitry required to operate the AD9653, AD9253 and AD9633 in their various modes and configurations. Figure 1 shows the typical bench characterization setup used to evaluate AC performance. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Getting Started section to get started, and visit UG-328 Design Support for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

Power Supplies

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to a 100 V ac to 240 V ac, 47 Hz to 63 Hz wall outlet. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P101. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, remove the E101, E102, E103 and E104 ferrite beads to disconnect the outputs from the

on-board LDOs. This enables the user to bias each section of the board individually. Use P102 and P103 to connect a different supply for each section. A 1.8 V, 0.5 A supply is needed for 1.8V_AVDD and 1.8V_DRVDD. Although the power supply requirements are the same for AVDD and DRVDD, it is recommended that separate supplies be used for both analog and digital domains. The SPI and its level shifters and alternate clock options require a separate 3.3 V, 0.5 A analog supply.

Two additional supplies, 5V_AVDD and 3V_AVDD, are used to bias the optional input path amplifiers and optional AD9517-3 clock chip. If used, these supplies should each have 0.5 A current capability.

Input Signals

When connecting the ADC clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA, or HP 8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multipole, narrow-band band-pass filter with 50 Ω terminations is recommended. Analog Devices uses band-pass filters from TTE and K&L Microwave, Inc. Connect the filters directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Analog Devices evaluation boards typically can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

Output Signals

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The serial LVDS outputs from the ADC are routed to Connector P1002 using 100 Ω differential traces. For more information on the data capture board and its optional settings, visit www.analog.com/hsadcevalboard.

Jumper Settings

Set the jumper settings/link options on the evaluation board for the required operating modes before powering on the board. The functions of the jumpers are described in Table 1. Figure 2 shows the default jumper settings.

Table 1. Jumper Settings

Jumper	Description

J202	This jumper selects between internal V_{REF} and external V_{REF}. To choose the internal 1 V reference, connect Pin 3 (DUT_SENSE) to Pin 5 (GND). To use the on-board ADR130 1 V reference, connect Pin 2 (DUT_SENSE) to Pin 1 (AVDD), and connect Pin 4 (DUT_VREF) to Pin 6 (EXT_REF). To apply a reference voltage from an external off-board source, connect Pin 2 (DUT_SENSE) to Pin 1 (AVDD) and apply the reference voltage to Pin 4 (DUT_VREF). The AD9653 can accommodate reference voltages from 1.0 V to 1.3 V; the AD9253 and AD9633 reference voltage is specified to be 1.0 V.
J204	Use this jumper to power down the ADC. Using the SPI, the PDWN pin can be configured to be STBY (standby).
J302	This jumper sets the ADC for SPI communications with the HSC-ADC-EVALCZ. Connect Pin 1 to Pin 2 for SDIO, Pin 4 to Pin 5 for SCLK, and Pin 8 to Pin 9 for CSB.
J803	This jumper enables the on-board crystal oscillator.

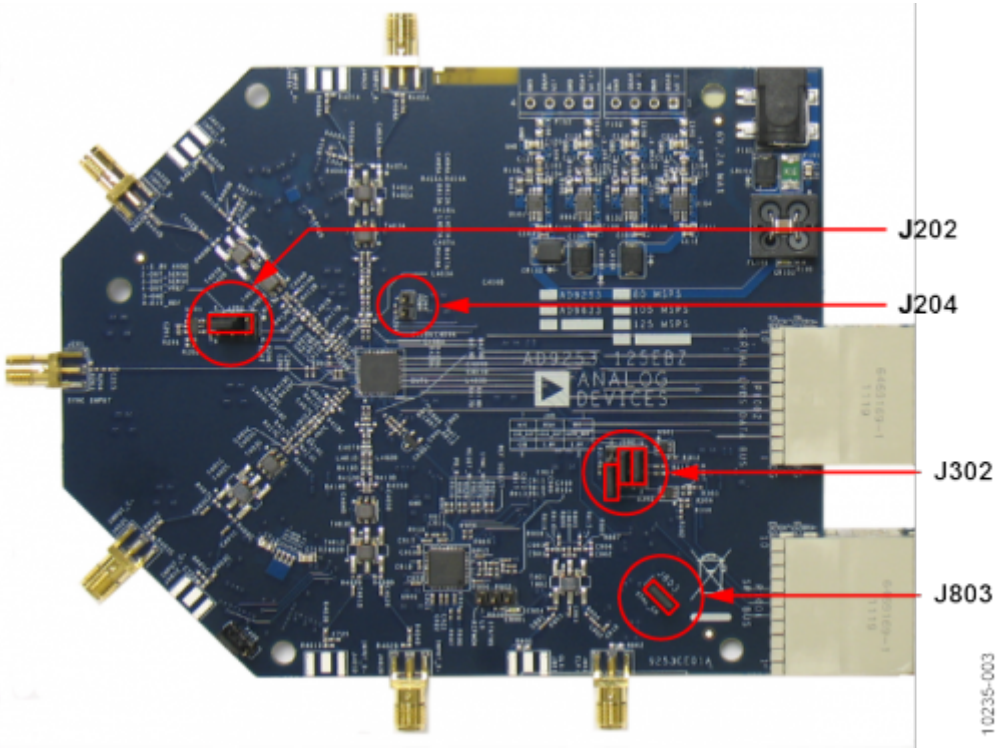


Figure 2. Default Jumper Connections for AD9653-125EBZ/AD9253-125EBZ/AD9633-125EBZ Board

Evaluation Board Circuitry

This section explains the default and optional settings or modes allowed on the AD9653-125EBZ, AD9253-125EBZ and the AD9633-125EBZ boards.

Power

Plug the switching power supply into a wall outlet rated at 100 V ac to 240 V ac, 47 Hz to 63 Hz. Connect the DC output connector to P101 on the evaluation board.

Analog Input

The four channel inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. The default analog input configuration supports analog input frequencies of up to ~200 MHz.

VREF

The default VREF configuration is to connect the SENSE pin to AGND for internal VREF operation. This is done by connecting Pin 3 to Pin 5 on Header J202. An external reference voltage can be provided to the AD9653, AD9253 and AD9633. Connecting Pin 2 to Pin 1 on Header J202 puts the ADC in a mode where it requires a reference voltage from an external source. The external on-board 1.0 V reference is provided by the ADR130. This external reference can be connected to the ADC by connecting Pin 4 to Pin 6 on Header J202. Alternatively, if an external off-board reference is desired, connect Pin 2 to Pin1 on Header J202 and apply the reference voltage directly to Pin 4 of Header J202. The AD9653 can accommodate reference voltages from 1.0 V to 1.3 V; the AD9253 and AD9633 reference voltage is specified to be 1.0 V.

RBIAS

RBIAS has a default setting of 10 kΩ (R205) to ground and is used to set the ADC core bias current. Note that using a resistor value other than a 10 kΩ, 1% resistor for RBIAS may degrade the performance of the device.

Clock

The default clock input circuit is derived from a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T801/T802) that adds a low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by

CR801 before entering the ADC clock inputs. The AD9653, AD9253 and AD9633 ADCs are equipped with an internal 8:1 clock divider to facilitate usage with higher frequency clocks. When using the internal divider and a higher input clock frequency, remove CR801 to preserve the slew rate of the clock signal.

The AD9653-125EBZ, AD9253-125EBZ and AD9633-125EBZ boards are set up to be clocked through the transformer-coupled input network from the crystal oscillator, Y801. This oscillator is a low phase noise oscillator from Valpey Fisher (VFAC3-BHL-125MHz). If a different clock source is desired, remove C810 (optional) and Jumper J803 to disable the oscillator from running and connect the external clock source to the SMA connector, J802 (labeled CLK+).

PDWN

To enable the power-down feature, add a shorting jumper across J204 at Pin 1 and Pin 2 to connect the PDWN pin to DRVDD.

Modes of Operation

Standalone (PIN) Mode

The AD9653/AD9253/AD9633 ADCs can operate in pin mode if there is no need to program and change the default modes of operation via the SPI. For applications that do not require SPI mode operation, the CSB pin is tied to AVDD, and the SDIO/OLM pin controls the output lane mode. Table 2 and Table 3 specify the settings for pin mode operation.

Table 2. Output Lane Mode (OLM) Pin Settings

OLM Pin Voltage	Output Mode
AVDD (Default)	Two-lane. 1× frame, 16-bit serial output
GND	One-lane. 1× frame, 16-bit serial output

Table 3. Digital Test Pattern (DTP) Pin Settings

Seected DTP	Output Mode	Resulting D0±x and D1±x
Normal Operation	10 kΩ to AGND	Normal operation
DTP	AVDD	1000 0000 0000 0000

Additional information on the lane modes is provided in the AD9653, AD9253 and AD9633 data sheets.

Default Mode

To operate the device under test (DUT) using the SPI, follow the jumper settings for J302 as shown in Table 1.

How To Use The Software For Testing

Setting up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 3, where the AD9253 is shown as an example).

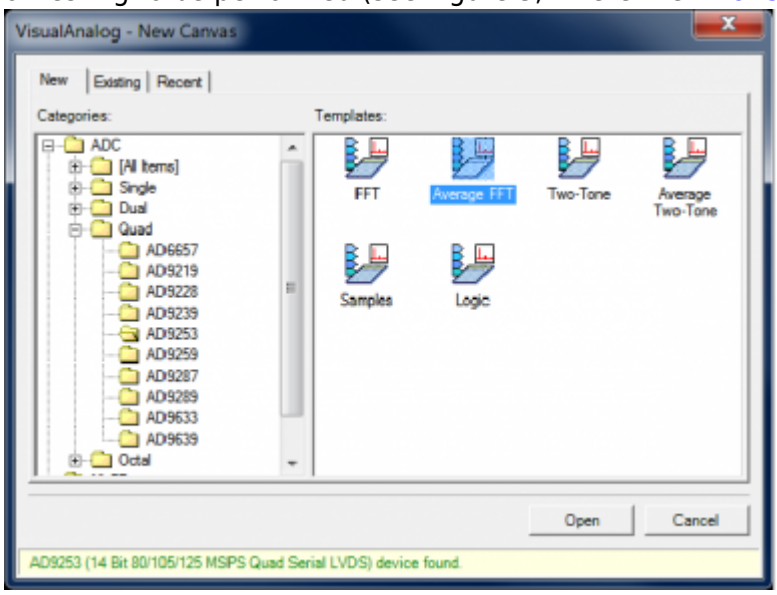


Figure 3. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 4). Click **Yes**, and the window closes.

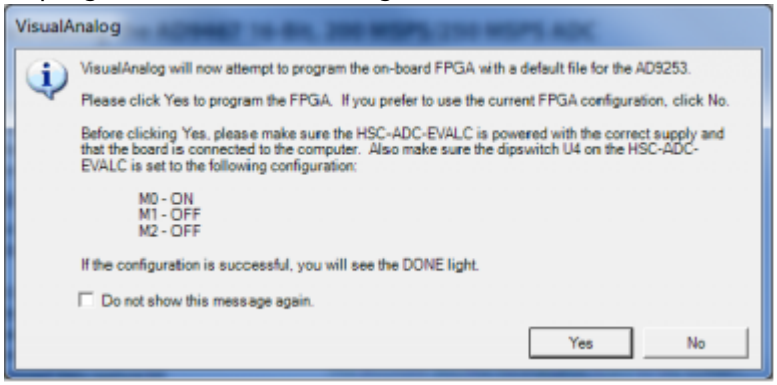


Figure 4. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button,

located on the bottom right corner of the window (see Figure 5), to see what is shown in Figure 6.

4. Change the features and capture settings by consulting the detailed instructions in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click the **Collapse Display** button.

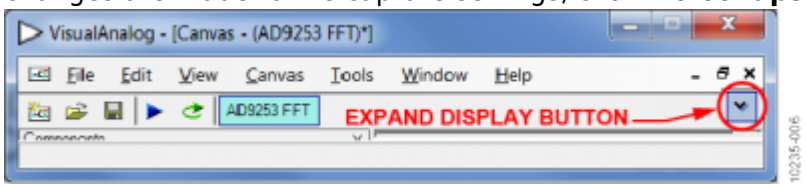


Figure 5. VisualAnalog Window Toolbar, Collapsed Display

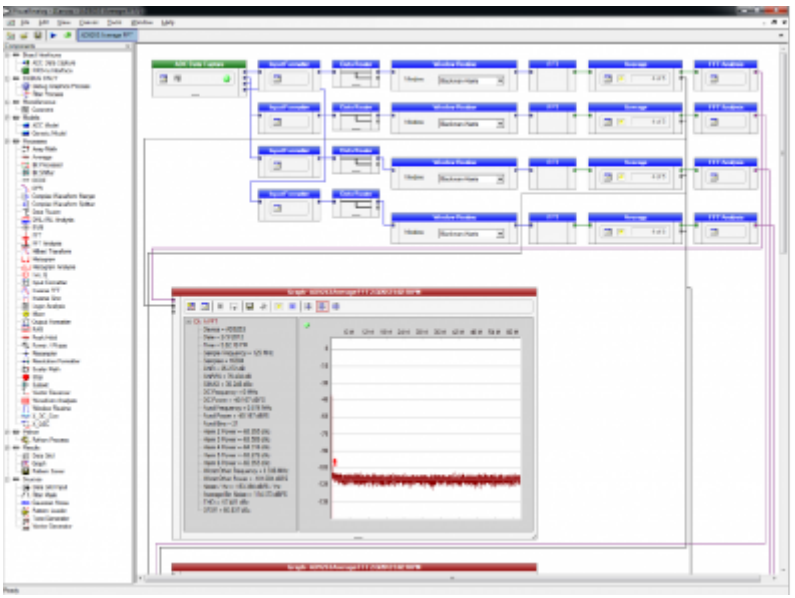


Figure 6. VisualAnalog, Main Window Expanded Display

Evaluation And Test

Setting up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI controller software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** box should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 7).

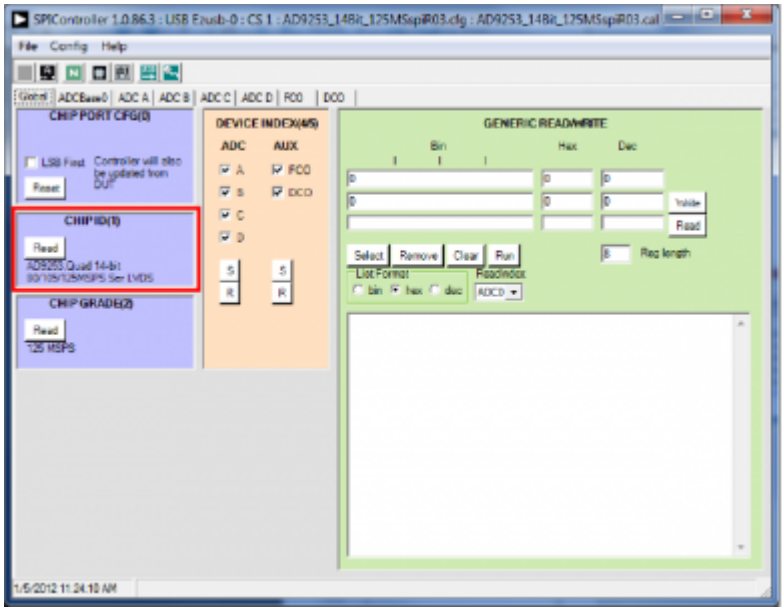


Figure 7. SPI Controller, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 8)

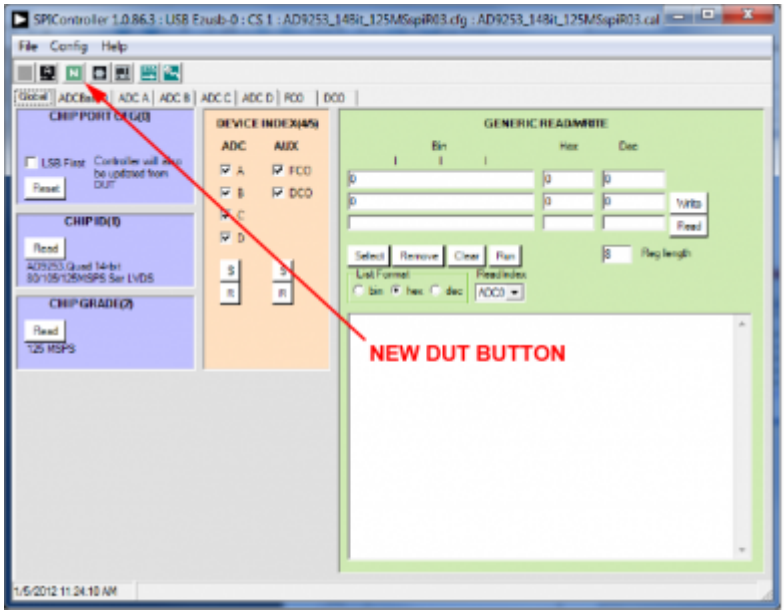
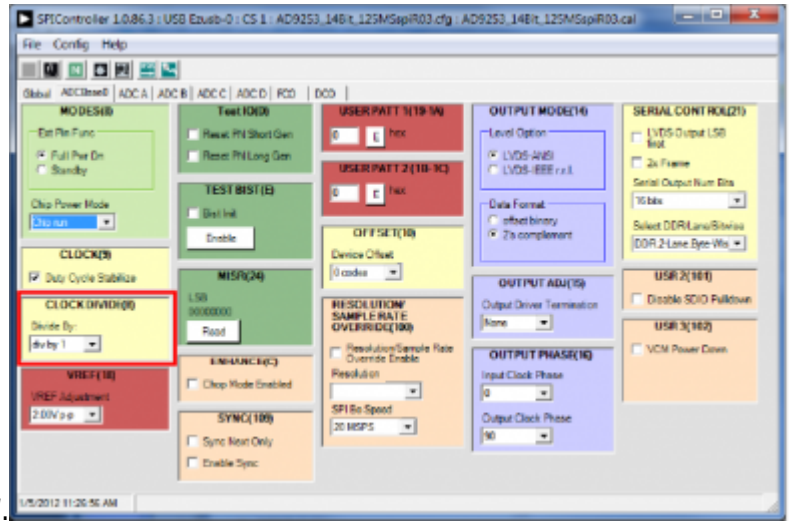


Figure 8. SPI Controller, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLOCK DIVIDE(B)** box (see Figure 9). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. For additional information, refer to the data sheet, the AN-878 Application Note, *High Speed ADC SPI Control Software*, and the AN-877 Application Note, *Interfacing to High Speed ADCs*



via SPI. *Figure 9. SPI Controller, CLOCK DIVIDE(B) Box*

4. Note that other settings can be changed on the **ADCBase 0 tab** (see Figure 9) and the **ADC A**, **ADC B**, **ADC C**, and **ADC D** tabs (see Figure 10) to set up the part in the desired mode. The **ADCBase 0** tab settings affect the entire part, whereas the settings on the **ADC A**, **ADC B**, **ADC C**, and **ADC D** tabs affect the selected channel only. See the appropriate part data sheet, the AN-878 Application Note, *High Speed ADC SPI Control Software*, and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

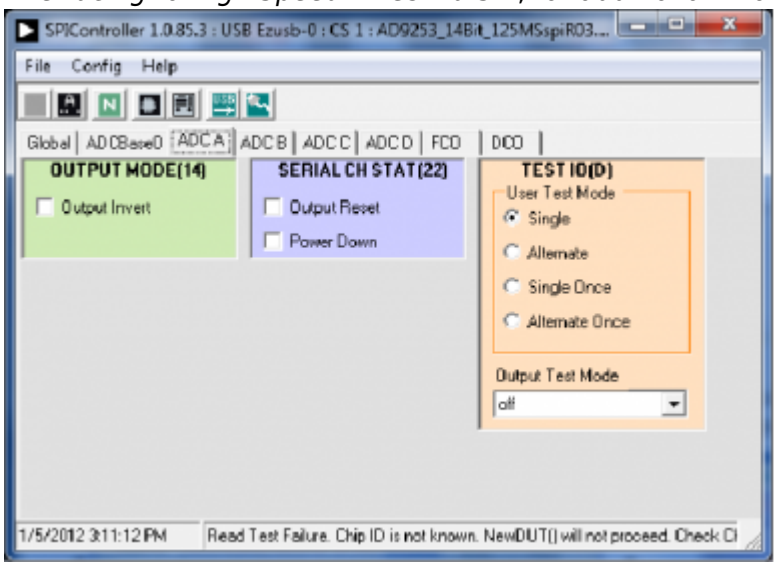


Figure 10. SPI Controller, Example ADC A Page

5. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 11).

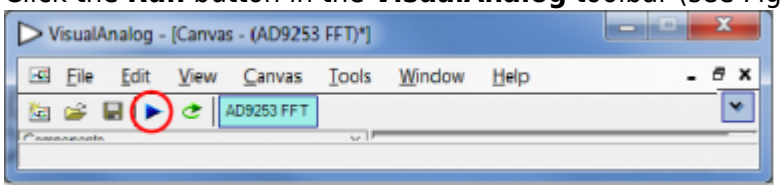


Figure 11. Run Button (Encircled in Red) in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. Examine the **Fund Power** reading in the left panel of the **VisualAnalog Graph - AD9253 FFT** window (see Figure 12).

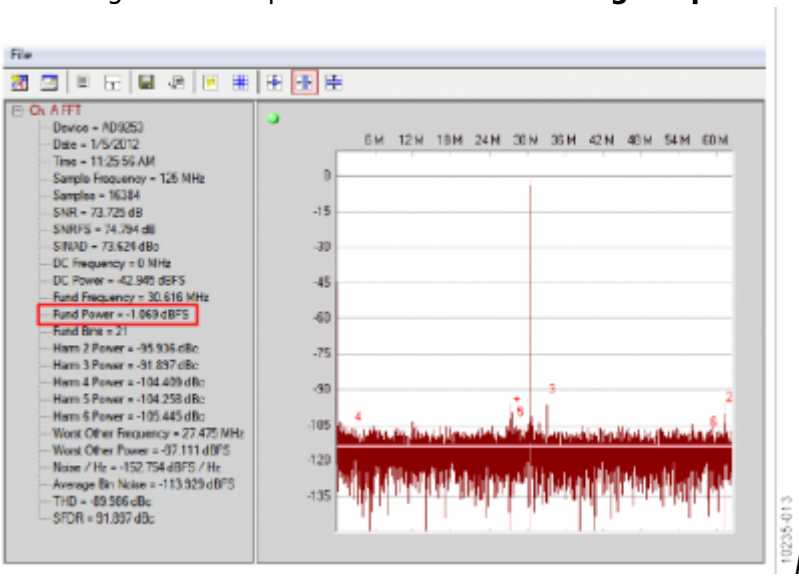


Figure 12. Graph Window of VisualAnalog

2. Repeat this procedure for Channel B, Channel C, and Channel D.
3. Click the disk icon within the **VisualAnalog Graph - AD9253 FFT** window to save the performance plot data as a .csv formatted file. See Figure 13 for an example.

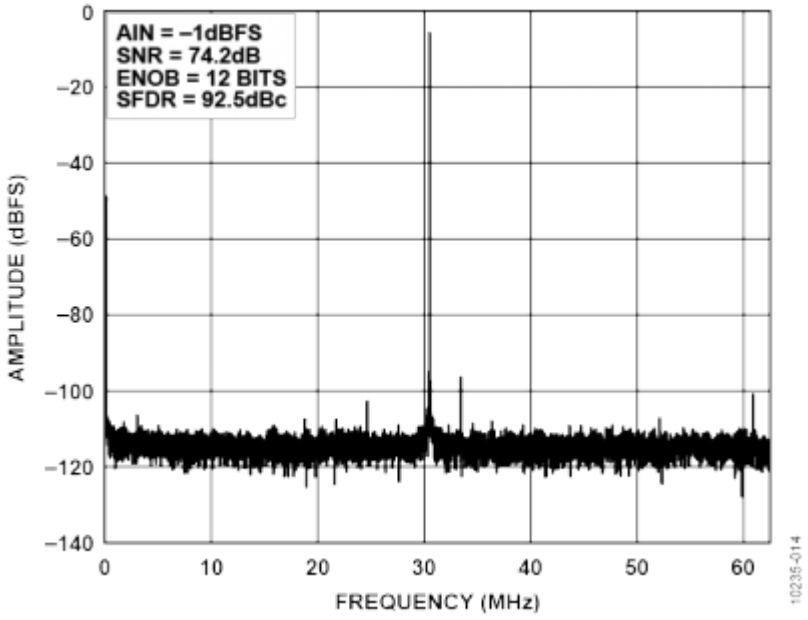


Figure 13. Typical FFT, AD9253

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see an abnormal noise floor, go to the **ADCBase0** tab of the **SPIController** window and toggle the **Chip Power Mode** in **MODES(8)** from **Chip Run** to **Reset** and back.
- If you see a normal noise floor when you disconnect the signal generator from the analog input, be

sure that you are not overdriving the ADC. Reduce the input level if necessary.
- In VisualAnalog, click the **Settings** icon in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (twos complement by default). Repeat for the other channels.

If the FFT appears normal but the performance is poor, check the following:

- Make sure that an appropriate filter is used on the analog input.
- Make sure that the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure that the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** in VisualAnalog (see Figure 11) is clicked, do the following:

- Make sure that the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure that the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure that the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure that the correct FPGA program was installed by clicking the **Settings** icon in the **ADC Data Capture** block in VisualAnalog. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If VisualAnalog indicates that the **FIFO Capture timed out**, do the following:

- Make sure that all power and USB connections are secure.
- Probe the DCO signal at P1002 (Pin A10 and/or Pin B10) on the evaluation board, and confirm that a clock signal is present at the ADC sampling rate.