

FEATURES

- 400MHz Gain Bandwidth Product
- 2500V/ μ s Slew Rate
- -85dBc Distortion at 5MHz
- 9mA Supply Current Per Amplifier
- Space Saving SOT-23 and MS8 Packages
- 6nV/ $\sqrt{\text{Hz}}$ Input Noise Voltage
- Unity-Gain Stable
- 1.5mV Maximum Input Offset Voltage
- 8 μ A Maximum Input Bias Current
- 800nA Maximum Input Offset Current
- 40mA Minimum Output Current, $V_{OUT} = \pm 3\text{V}$
- $\pm 3.5\text{V}$ Minimum Input CMR, $V_S = \pm 5\text{V}$
- Specified at $\pm 5\text{V}$, Single 5V Supplies
- Operating Temperature Range: -40°C to 85°C

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Communication Receivers
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

The LT[®]1818/LT1819 are single/dual wide bandwidth, high slew rate, low noise and distortion operational amplifiers with excellent DC performance. The LT1818/LT1819 have been designed for wider bandwidth and slew rate, much lower input offset voltage and lower noise and distortion than devices with comparable supply current. The circuit topology is a voltage feedback amplifier with the excellent slewing characteristics of a current feedback amplifier.

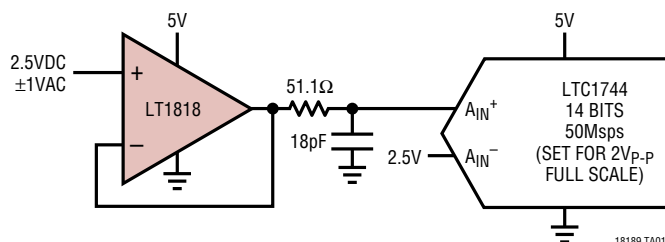
The output drives a 100 Ω load to $\pm 3.8\text{V}$ with $\pm 5\text{V}$ supplies. On a single 5V supply, the output swings from 1V to 4V with a 100 Ω load connected to 2.5V. The amplifier is unity-gain stable with a 20pF capacitive load without the need for a series resistor. Harmonic distortion is -85dBc up to 5MHz for a 2V_{P-P} output at a gain of 2.

The LT1818/LT1819 are manufactured on Linear Technology's advanced low voltage complementary bipolar process. The LT1818 (single op amp) is available in SOT-23 and SO-8 packages; the LT1819 (dual op amp) is available in MSOP-8 and SO-8 packages.

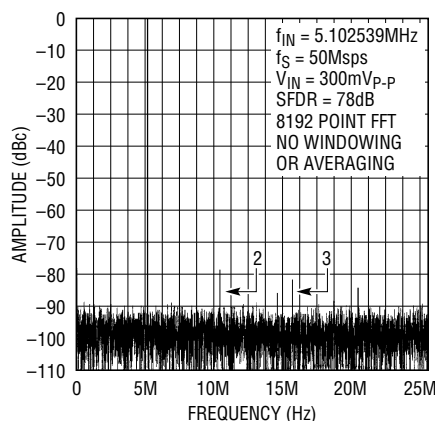
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TYPICAL APPLICATION

Single Supply Unity-Gain ADC Driver for Oversampling Applications



FFT of Single Supply ADC Driver



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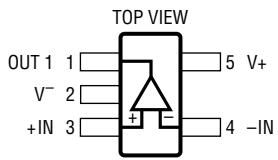
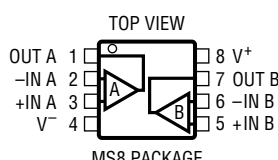
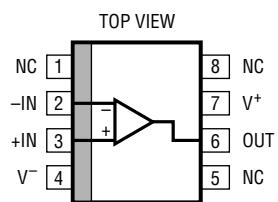
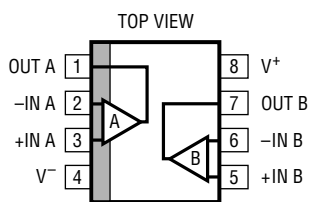
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
 Differential Input Voltage
 (Transient Only, Note 2) $\pm 6V$
 Output Short-Circuit Duration (Note 3) Indefinite
 Operating Temperature Range (Note 8) .. -40°C to 85°C

Specified Temperature Range (Note 9) ... -40°C to 85°C
 Maximum Junction Temperature 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

 S5 PACKAGE 5-LEAD PLASTIC SOT-23 $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 250^\circ\text{C/W}$ (NOTE 10)	ORDER PART NUMBER	 MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 250^\circ\text{C/W}$ (NOTE 10)	ORDER PART NUMBER
	LT1818CS5 LT1818IS5		LT1819CMS8 LT1819IMS8
	S5 PART* MARKING		MS8 PART MARKING
 S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$ (NOTE 10)	ORDER PART NUMBER	 S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$ (NOTE 10)	ORDER PART NUMBER
	LT1818CS8 LT1818IS8		LT1819CS8 LT1819IS8
	S8 PART MARKING		S8 PART MARKING
	1818 1818I		1819 1819I

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 9) $V_S = \pm 5V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.2	1.5	mV
		$T_A = 0^\circ\text{C}$ to 70°C	●		2.0	mV
		$T_A = -40^\circ\text{C}$ to 85°C	●		3.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	$T_A = 0^\circ\text{C}$ to 70°C (Note 7)	●	10	15	$\mu\text{V}/^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to 85°C (Note 7)	●	10	30	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$T_A = 0^\circ\text{C}$ to 70°C	●	60	800	nA
		$T_A = -40^\circ\text{C}$ to 85°C	●		1000	nA
					1200	nA
I_B	Input Bias Current	$T_A = 0^\circ\text{C}$ to 70°C	●	-2	± 8	μA
		$T_A = -40^\circ\text{C}$ to 85°C	●		± 10	μA
			●		± 12	μA
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.2		$\text{pA}/\sqrt{\text{Hz}}$

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 9) $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	$V_{CM} = V^- + 1.5\text{V}$ to $V^+ - 1.5\text{V}$ Differential	1.5	5 750		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance			1.5		pF
V_{CM}	Input Voltage Range (Positive/Negative)	Guaranteed by CMRR $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.5 ● ± 3.5	± 4.2		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 75 ● 73 ● 72	85		dB dB dB
	Minimum Supply Voltage	Guaranteed by PSRR $T_A = -40^\circ\text{C}$ to 85°C	●	± 1.25	± 2 ± 2	V V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2\text{V}$ to $\pm 5.5\text{V}$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 78 ● 76 ● 75	97		dB dB dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 3\text{V}$, $R_L = 500\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 1.5 ● 1.0 ● 0.8	2.5		V/mV V/mV V/mV
		$V_{OUT} = \pm 3\text{V}$, $R_L = 100\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 1.0 ● 0.7 ● 0.6	6		V/mV V/mV V/mV
	Channel Separation	$V_{OUT} = \pm 3\text{V}$, LT1819 $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 82 ● 81 ● 80	100		dB dB dB
V_{OUT}	Output Swing (Positive/Negative)	$R_L = 500\Omega$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.8 ● ± 3.7 ● ± 3.6	± 4.1		V V V
		$R_L = 100\Omega$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 3.50 ● ± 3.25 ● ± 3.15	± 3.8		V V V
I_{OUT}	Output Current	$V_{OUT} = \pm 3\text{V}$, 30mV Overdrive $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 40 ● ± 35 ● ± 30	± 70		mA mA mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0\text{V}$, 1V Overdrive (Note 3) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ± 100 ● ± 90 ● ± 70	± 200		mA mA mA
SR	Slew Rate	$A_V = 1$		2500		V/ μs
		$A_V = -1$ (Note 5) $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 900 ● 750 ● 600	1800		V/ μs V/ μs V/ μs
FPBW	Full Power Bandwidth	$6V_{P-P}$ (Note 6)		95		MHz
GBW	Gain Bandwidth Product	$f = 4\text{MHz}$, $R_L = 500\Omega$ $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● 270 ● 260 ● 250	400		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V Step		0.6		ns
t_{PD}	Propagation Delay	$A_V = 1$, 50% to 50%, 0.1V Step		1.0		ns
OS	Overshoot	$A_V = 1$, 0.1V, $R_L = 100\Omega$		20		%
t_S	Settling Time	$A_V = -1$, 0.1%, 5V		10		ns
HD	Harmonic Distortion	HD2, $A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-85		dBc
		HD3, $A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-89		dBc
dG	Differential Gain	$A_V = 2$, $R_L = 150\Omega$		0.07		%
dP	Differential Phase	$A_V = 2$, $R_L = 150\Omega$		0.02		DEG
I_S	Supply Current	Per Amplifier $T_A = 0^\circ\text{C}$ to 70°C $T_A = -40^\circ\text{C}$ to 85°C	● ● ●	9	10 13 14	mA mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 9). $V_S = 5\text{V}$, 0V ; $V_{CM} = 2.5\text{V}$, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.4	2.0	mV
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●		2.5	mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		3.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	15	$\mu\text{V}/^\circ\text{C}$
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	10	30	$\mu\text{V}/^\circ\text{C}$
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●			
I_{OS}	Input Offset Current	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	60	800	nA
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		1000	nA
					1200	nA
I_B	Input Bias Current	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	-2.4	± 8	μA
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		± 10	μA
					± 12	μA
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.4		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = V^- + 1.5\text{V to } V^+ - 1.5\text{V}$		1.5	5	M Ω
		Differential			750	k Ω
C_{IN}	Input Capacitance			1.5		pF
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR $T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	3.5	4.2	V
	Input Voltage Range (Negative)	Guaranteed by CMRR $T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		0.8	1.5
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5\text{V to } 3.5\text{V}$		73	82	dB
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	71		dB
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	70		dB
	Minimum Supply Voltage	Guaranteed by PSRR $T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	± 1.25	± 2	V
					± 2	V
PSRR	Power Supply Rejection Ratio	$V_S = 4\text{V to } 11\text{V}$		78	97	dB
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	76		dB
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	75		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5\text{V to } 3.5\text{V}$, $R_L = 500\Omega$		1.0	2	V/mV
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	0.7		V/mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	0.6		V/mV
		$V_{OUT} = 1.5\text{V to } 3.5\text{V}$, $R_L = 100\Omega$		0.7	4	V/mV
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	0.5		V/mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	0.4		V/mV
	Channel Separation	$V_{OUT} = 1.5\text{V to } 3.5\text{V}$, LT1819		81	100	dB
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	80		dB
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	79		dB
V_{OUT}	Output Swing(Positive)	$R_L = 500\Omega$, 30mV Overdrive		3.9	4.2	V
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	3.8		V
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	3.7		V
		$R_L = 100\Omega$, 30mV Overdrive		3.7	4	V
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●	3.6		V
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●	3.5		V
	Output Swing(Negative)	$R_L = 500\Omega$, 30mV Overdrive		0.8	1.1	V
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●		1.2	V
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		1.3	V
		$R_L = 100\Omega$, 30mV Overdrive		1	1.3	V
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	●		1.4	V
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	●		1.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 9). $V_S = 5\text{V}$, 0V ; $V_{CM} = 2.5\text{V}$, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = 1.5\text{V}$ or 3.5V , 30mV Overdrive		± 30	± 50	mA
		$T_A = 0^\circ\text{C}$ to 70°C	●	± 25		mA
		$T_A = -40^\circ\text{C}$ to 85°C	●	± 20		mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 2.5\text{V}$, 1V Overdrive (Note 3)		± 80	± 140	mA
		$T_A = 0^\circ\text{C}$ to 70°C	●	± 70		mA
		$T_A = -40^\circ\text{C}$ to 85°C	●	± 50		mA
SR	Slew Rate	$A_V = 1$		1000		V/ μs
		$A_V = -1$ (Note 5)		450	800	V/ μs
		$T_A = 0^\circ\text{C}$ to 70°C	●	375		V/ μs
		$T_A = -40^\circ\text{C}$ to 85°C	●	300		V/ μs
FPBW	Full Power Bandwidth	$2V_{P-P}$ (Note 6)		125		MHz
GBW	Gain Bandwidth Product	$f = 4\text{MHz}$, $R_L = 500\Omega$		240	360	MHz
		$T_A = 0^\circ\text{C}$ to 70°C	●	230		MHz
		$T_A = -40^\circ\text{C}$ to 85°C	●	220		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V Step		0.7		ns
t_{PD}	Propagation Delay	$A_V = 1$, 50% to 50%, 0.1V Step		1.1		ns
OS	Overshoot	$A_V = 1$, 0.1V, $R_L = 100\Omega$		20		%
HD	Harmonic Distortion	HD2, $A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-72		dBc
		HD3, $A_V = 2$, $f = 5\text{MHz}$, $V_{OUT} = 2V_{P-P}$, $R_L = 500\Omega$		-74		dBc
dG	Differential Gain	$A_V = 2$, $R_L = 150\Omega$		0.07		%
dP	Differential Phase	$A_V = 2$, $R_L = 150\Omega$		0.07		DEG
I_S	Supply Current	Per Amplifier		8.5	10	mA
		$T_A = 0^\circ\text{C}$ to 70°C	●		13	mA
		$T_A = -40^\circ\text{C}$ to 85°C	●		14	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of $\pm 6\text{V}$ are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: With $\pm 5\text{V}$ supplies, slew rate is tested in a closed-loop gain of -1 by measuring the rise time of the output from -2V to 2V with an output step from -3V to 3V . With single 5V supplies, slew rate is tested in a closed-loop gain of -1 by measuring the rise time of the output from 1.5V to 3.5V with an output step from 1V to 4V . Falling edge slew rate is not production tested, but is designed, characterized and expected to be within 10% of the rising edge slew rate.

Note 6: Full power bandwidth is calculated from the slew rate:

$$\text{FPBW} = \text{SR}/2\pi V_P$$

Note 7: This parameter is not 100% tested.

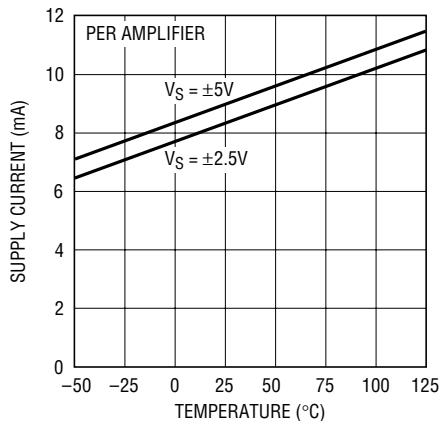
Note 8: The LT1818C/LT1818I and LT1819C/LT1819I are guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 9: The LT1818C/LT1819C are guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet the extended temperature limits, but is not tested at -40°C and 85°C . The LT1818I/LT1819I are guaranteed to meet the extended temperature limits.

Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be significantly reduced by connecting the V^- pin to a large metal area.

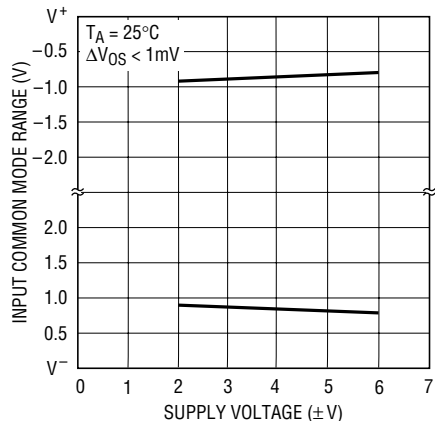
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



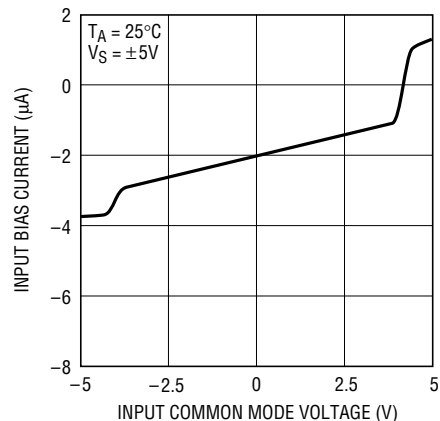
18189 G01

Input Common Mode Range vs Supply Voltage



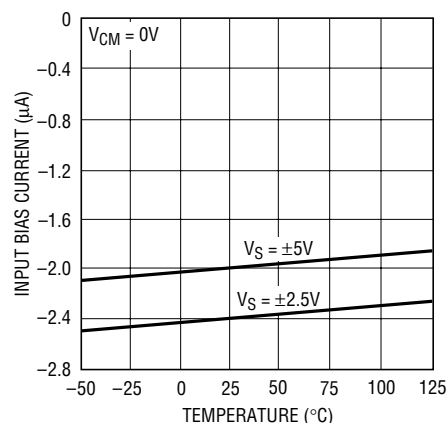
18189 G02

Input Bias Current vs Common Mode Voltage



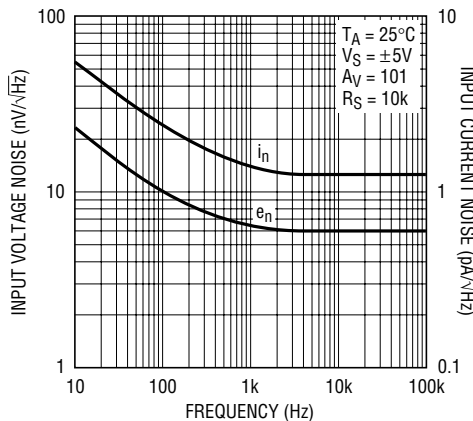
18189 G03

Input Bias Current vs Temperature



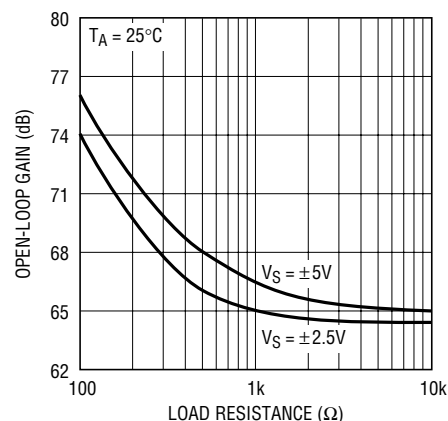
18189 G04

Input Noise Spectral Density



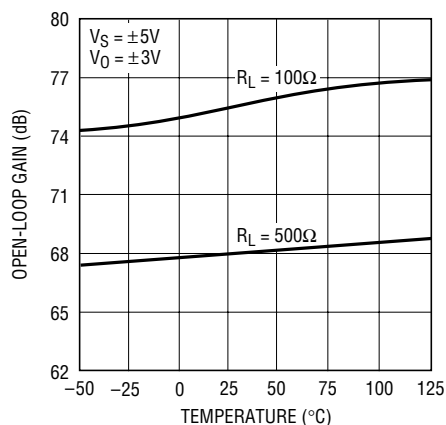
18189 G05

Open-Loop Gain vs Resistive Load



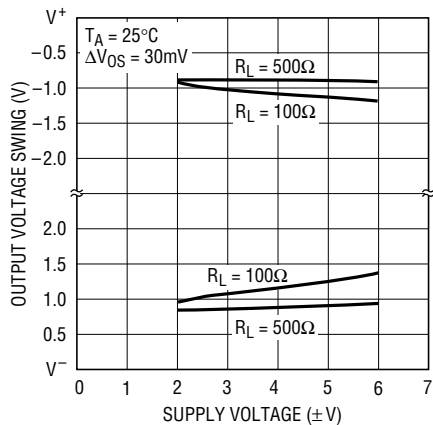
18189 G06

Open-Loop Gain vs Temperature



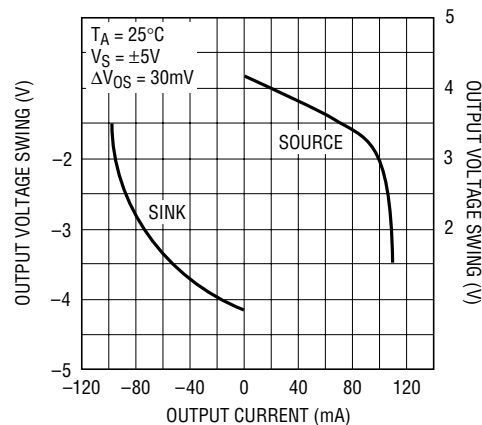
18189 G07

Output Voltage Swing vs Supply Voltage



18189 G08

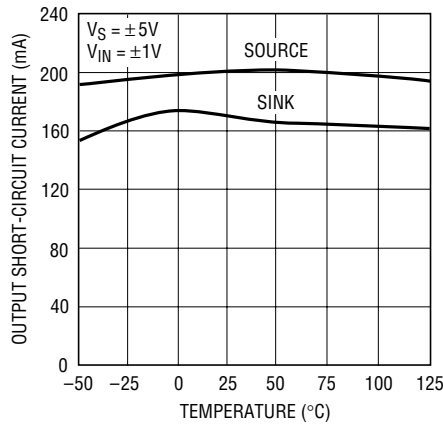
Output Voltage Swing vs Load Current



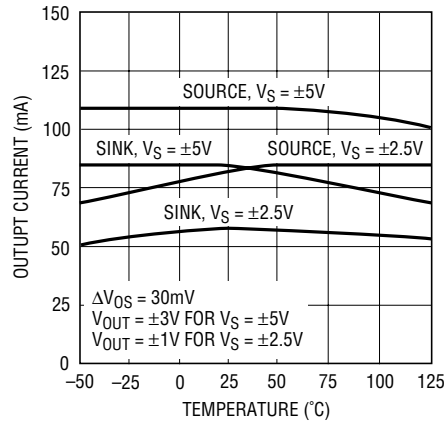
18189 G09

TYPICAL PERFORMANCE CHARACTERISTICS

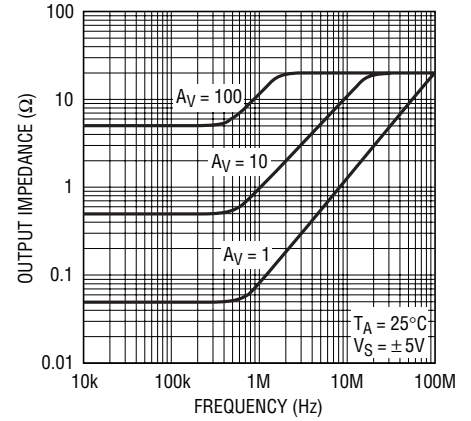
Output Short-Circuit Current vs Temperature



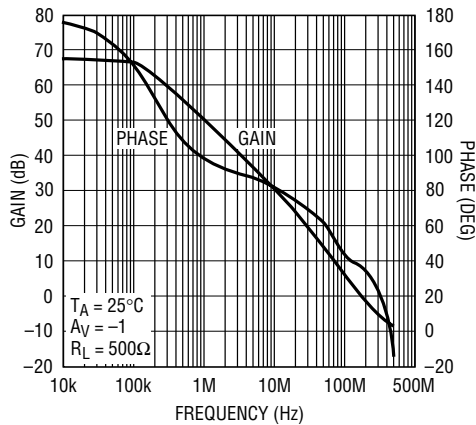
Output Current vs Temperature



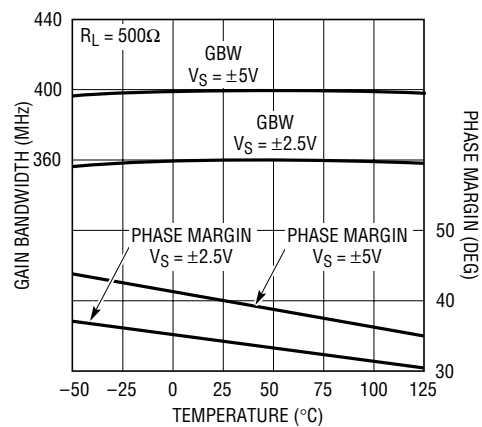
Output Impedance vs Frequency



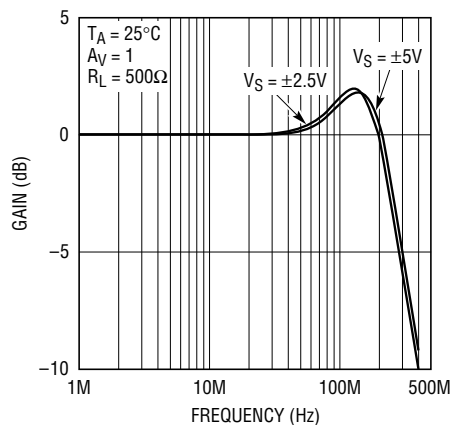
Gain and Phase vs Frequency



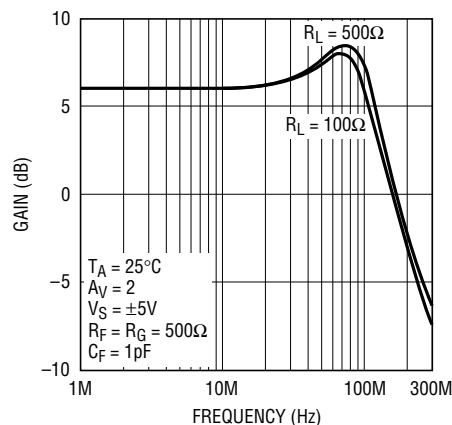
Gain Bandwidth and Phase Margin vs Temperature



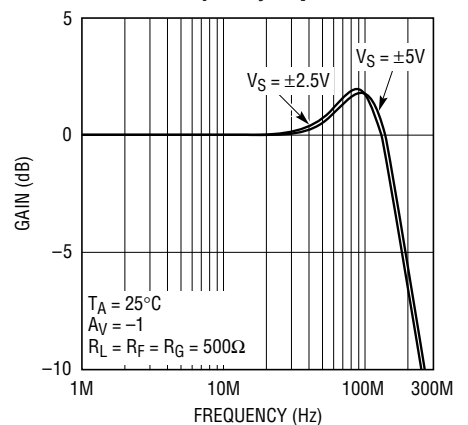
Gain vs Frequency, $A_V = 1$



Gain vs Frequency, $A_V = 2$

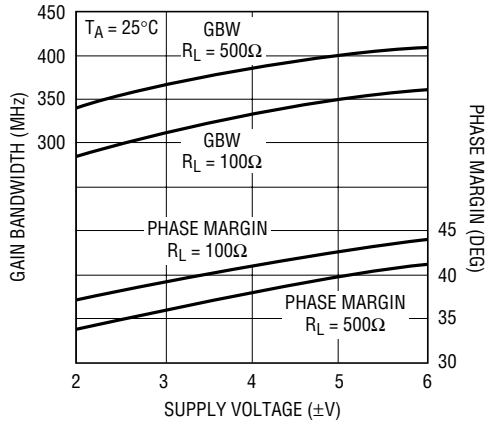


Gain vs Frequency, $A_V = -1$

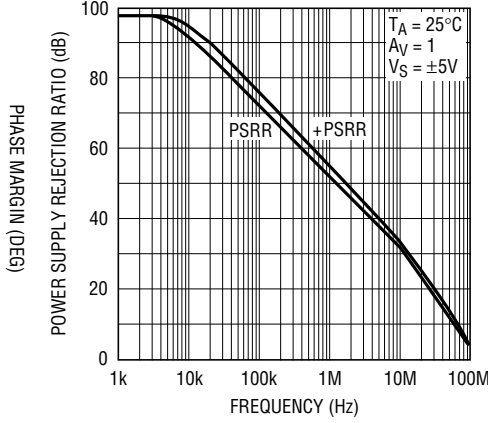


TYPICAL PERFORMANCE CHARACTERISTICS

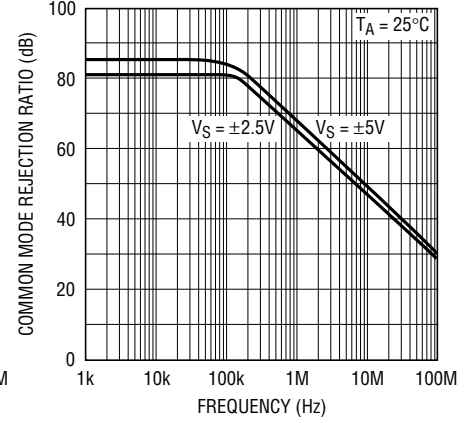
Gain Bandwidth and Phase Margin vs Supply Voltage



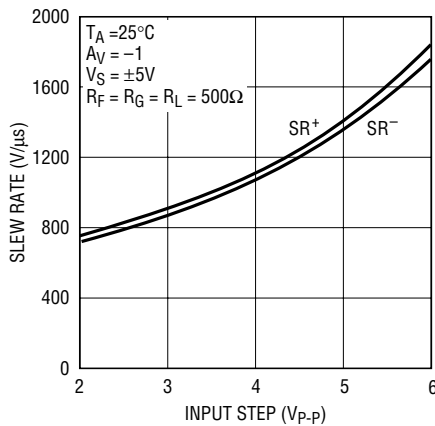
Power Supply Rejection Ratio vs Frequency



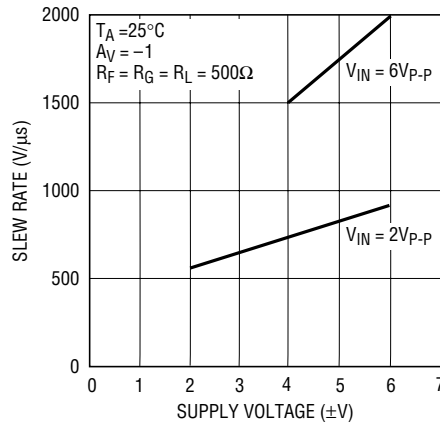
Common Mode Rejection Ratio vs Frequency



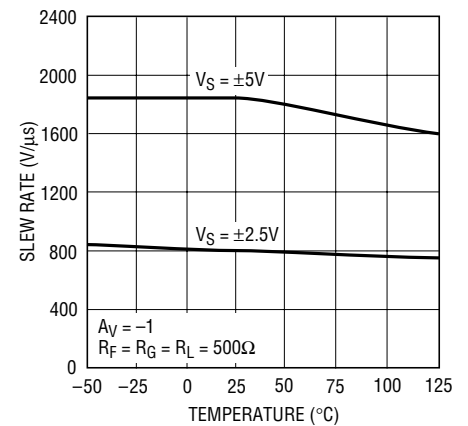
Slew Rate vs Input Step



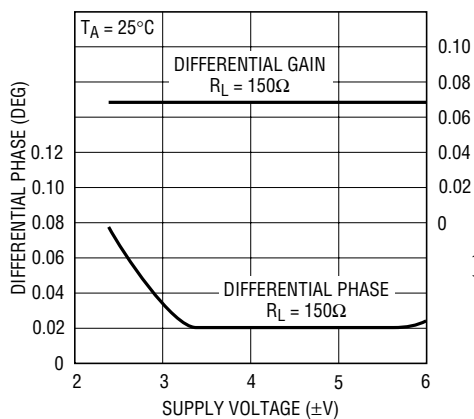
Slew Rate vs Supply Voltage



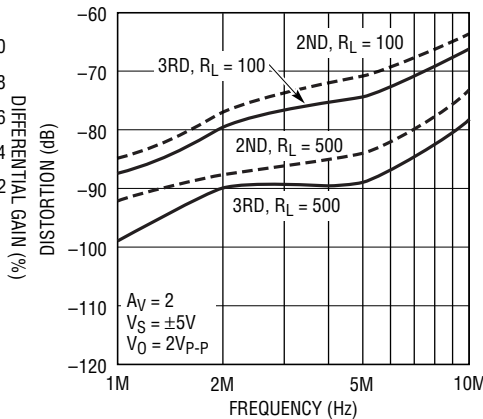
Slew Rate vs Temperature



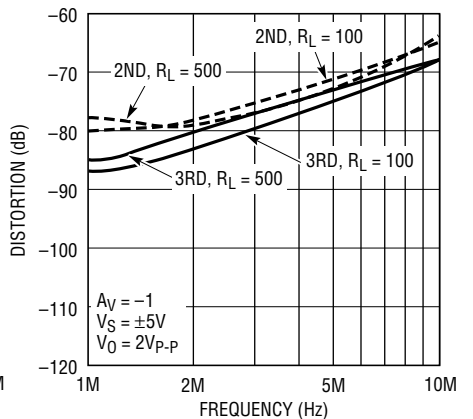
Differential Gain and Phase vs Supply Voltage



Distortion vs Frequency, AV = 2

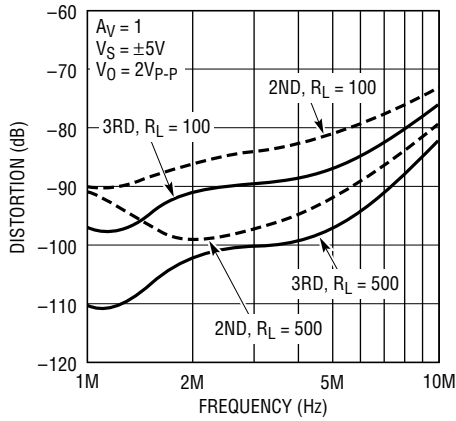


Distortion vs Frequency, AV = -1

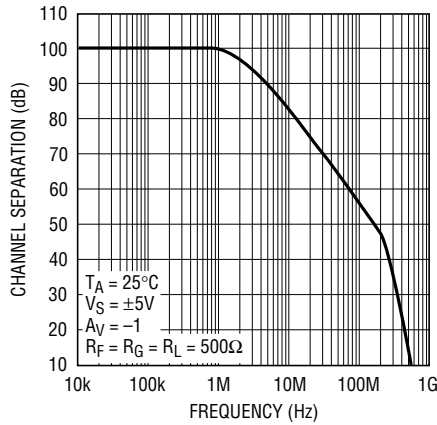


TYPICAL PERFORMANCE CHARACTERISTICS

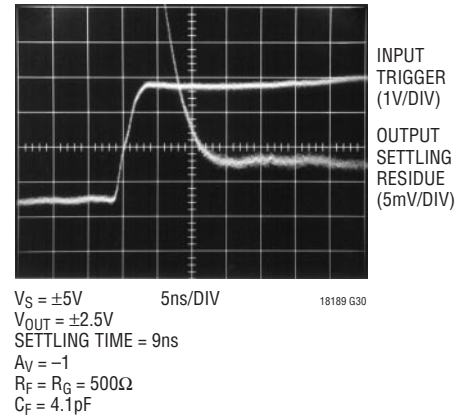
Distortion vs Frequency, $A_V = 1$



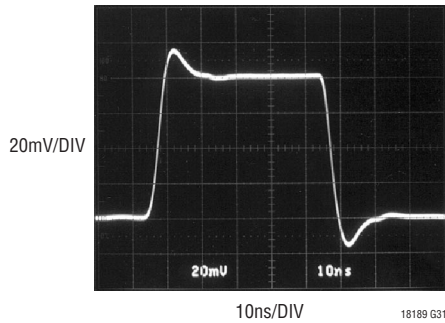
Channel Separation vs Frequency



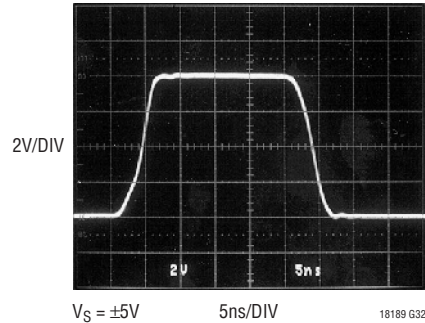
0.1% Settling Time



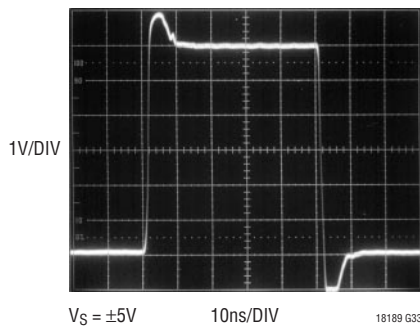
Small-Signal Transient, 20dB Gain



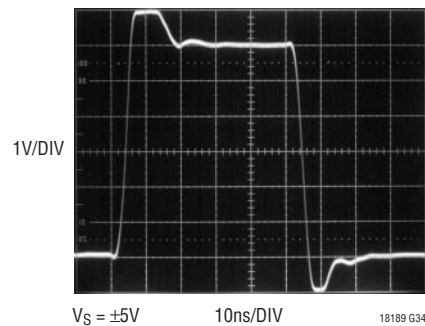
Large-Signal Transient, $A_V = -1$



Large-Signal Transient, $A_V = 1$



Large-Signal Transient, $A_V = -1$



APPLICATIONS INFORMATION

Layout and Passive Components

As with all high speed amplifiers, the LT1818/LT1819 require some attention to board layout. A ground plane is recommended and trace lengths should be minimized, especially on the negative input lead.

Low ESL/ESR bypass capacitors should be placed directly at the positive and negative supply (0.01μF ceramics are recommended). For high drive current applications, additional 1μF to 10μF tantalums should be added.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 500Ω are used, a parallel capacitor of value

$$C_F > R_G \cdot C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance (see Figure 1). For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be an I-to-V converter.

In high closed-loop gain configurations, $R_F \gg R_G$, and no C_F need to be added. To optimize the bandwidth in these applications, a capacitance, C_G , may be added in parallel with R_G in order to cancel out any parasitic C_F capacitance.

Capacitive Loading

The LT1818/LT1819 are optimized for low distortion and high gain bandwidth applications. The amplifiers can drive a capacitive load of 20pF in a unity-gain configuration and more with higher gain. When driving a larger capacitive

load, a resistor of 10Ω to 50Ω must be connected between the output and the capacitive load to avoid ringing or oscillation (see R_S in Figure 1). The feedback must still be taken directly from the output so that the series resistor will isolate the capacitive load to ensure stability.

Input Considerations

The inputs of the LT1818/LT1819 amplifiers are connected to the bases of NPN and PNP bipolar transistors in parallel. The base currents are of opposite polarity and provide first order bias current cancellation. Due to variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current, however, does not depend on beta matching and is tightly controlled. Therefore, the use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. For example, with a 100Ω source resistance at each input, the 800nA maximum offset current results in only 80μV of extra offset, while without balance the 8μA maximum input bias current could result in an 0.8mV offset condition.

The inputs can withstand differential input voltages of up to 6V without damage and without needing clamping or series resistance for protection. This differential input voltage generates a large internal current (up to 50mA), which results in the high slew rate. In normal transient closed-loop operation, this does not increase power dissipation significantly because of the low duty cycle of the transient inputs. Sustained differential inputs, however, will result in excessive power dissipation and therefore **this device should not be used as a comparator.**

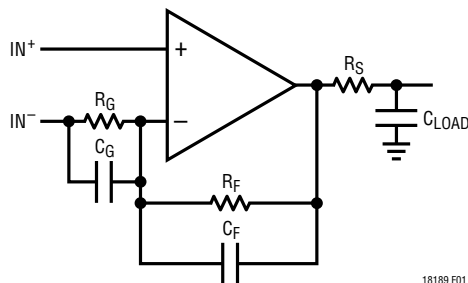


Figure 1

APPLICATIONS INFORMATION

Slew Rate

The slew rate of the LT1818/LT1819 is proportional to the differential input voltage. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 6V output step with a gain of 10 has a 0.6V input step, whereas at unity gain there is a 6V input step. The LT1818/LT1819 is tested for slew rate at a gain of -1 . Lower slew rates occur in higher gain configurations, whereas the highest slew rate (2500V/ μ s) occurs in a noninverting unity-gain configuration.

Power Dissipation

The LT1818/LT1819 combine high speed and large output drive in small packages. It is possible to exceed the maximum junction temperature specification (150°C) under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A), power dissipation per amplifier (P_D) and number of amplifiers (n) as follows:

$$T_J = T_A + (n \cdot P_D \cdot \theta_{JA})$$

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The worst-case load-induced power occurs when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 the supply voltage). Therefore $P_{D\text{MAX}}$ is:

$$P_{D\text{MAX}} = (V^+ - V^-) \cdot (I_{S\text{MAX}}) + (V^+/2)^2/R_L \text{ or}$$

$$P_{D\text{MAX}} = (V^+ - V^-) \cdot (I_{S\text{MAX}}) + (V^+ - V_{O\text{MAX}}) \cdot (V_{O\text{MAX}}/R_L)$$

Example: LT1819IS8 at 85°C, $V_S = \pm 5V$, $R_L = 100\Omega$

$$P_{D\text{MAX}} = (10V) \cdot (14mA) + (2.5V)^2/100\Omega = 202.5mW$$

$$T_{J\text{MAX}} = 85^\circ\text{C} + (2 \cdot 202.5mW) \cdot (150^\circ\text{C/W}) = 146^\circ\text{C}$$

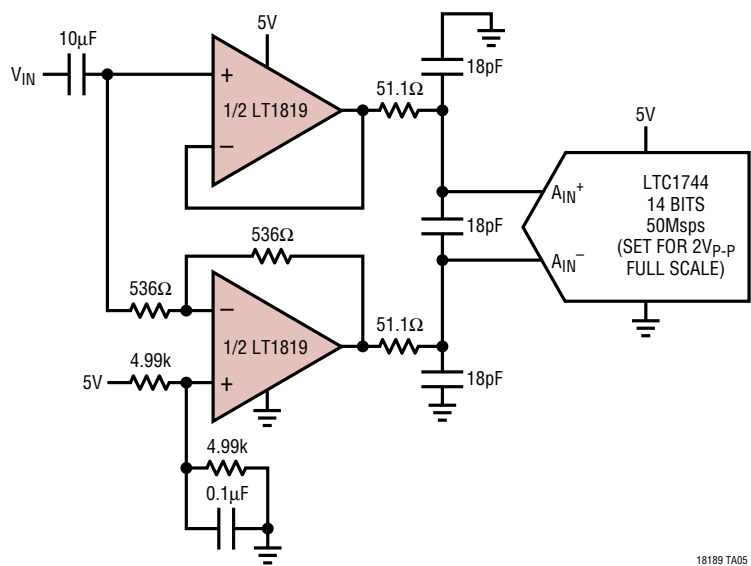
Circuit Operation

The LT1818/LT1819 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. Complementary NPN and PNP emitter followers buffer the inputs and drive an internal resistor. The input voltage appears across the resistor, generating a current that is mirrored into the high impedance node.

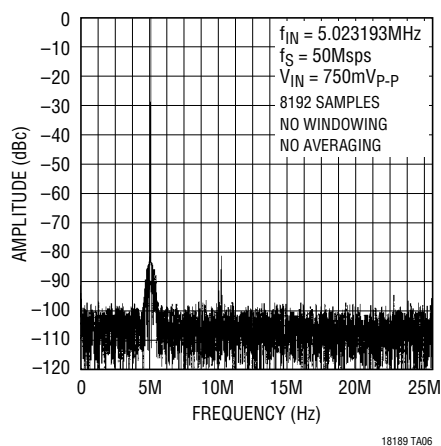
Complementary followers form an output stage that buffer the gain node from the load. The input resistor, input stage transconductance and the capacitor on the high impedance node determine the bandwidth. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R_1 , so the slew rate is proportional to the input step. Highest slew rates are therefore seen in the lowest gain configurations.

TYPICAL APPLICATION

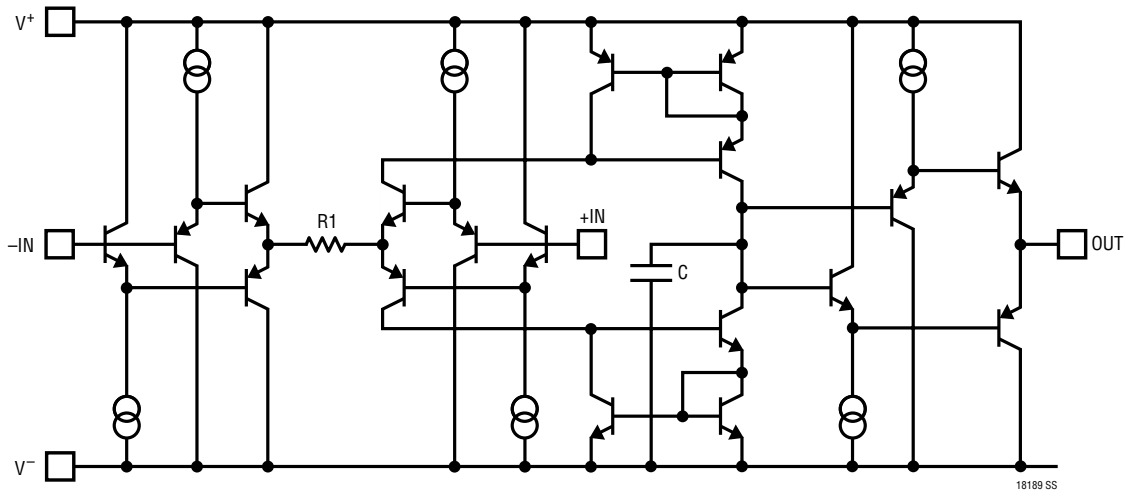
Single Supply Differential ADC Driver



Results Obtained with the Circuit of Figure 2 at 5MHz.
FFT Shows 81dB Overall Spurious Free Dynamic Range

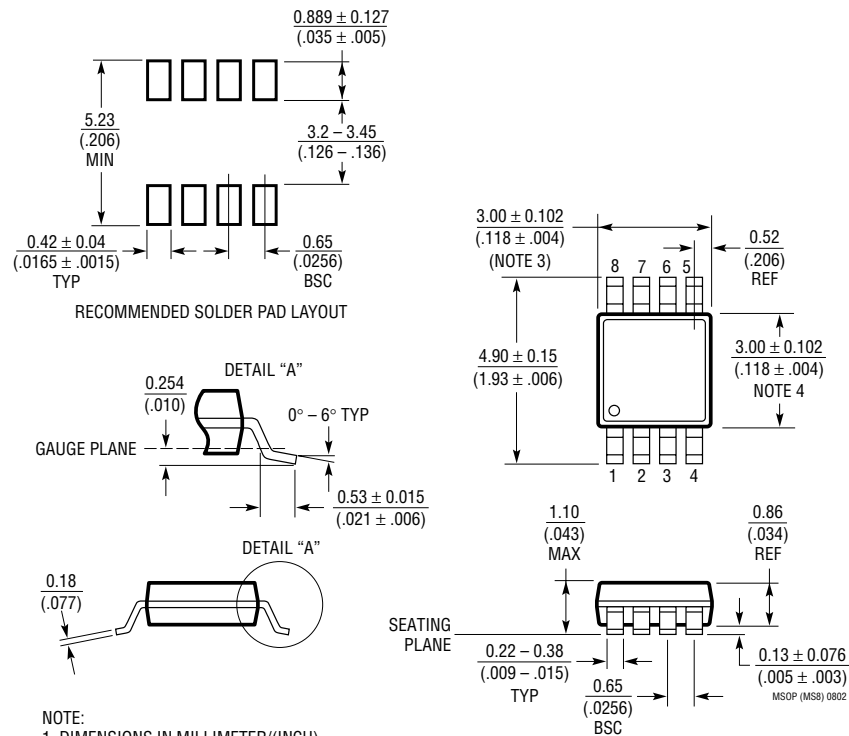


SIMPLIFIED SCHEMATIC (One Amplifier)



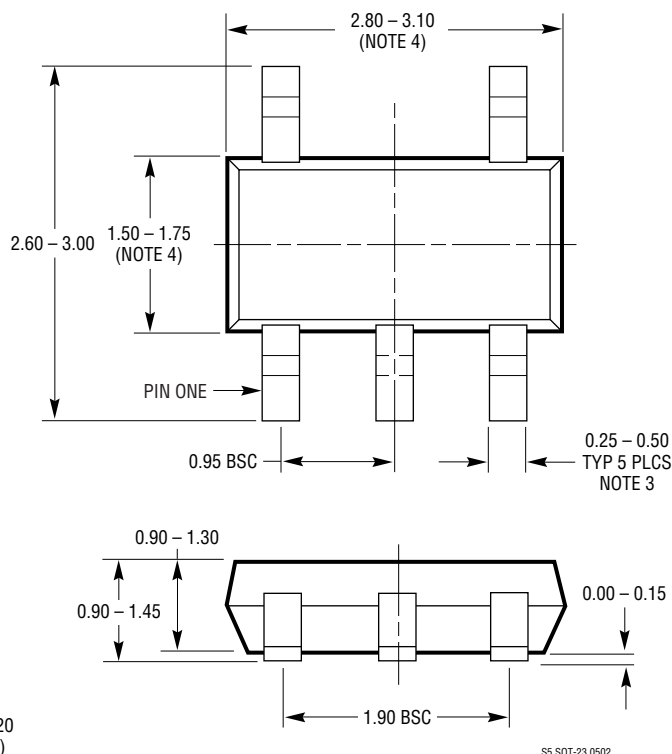
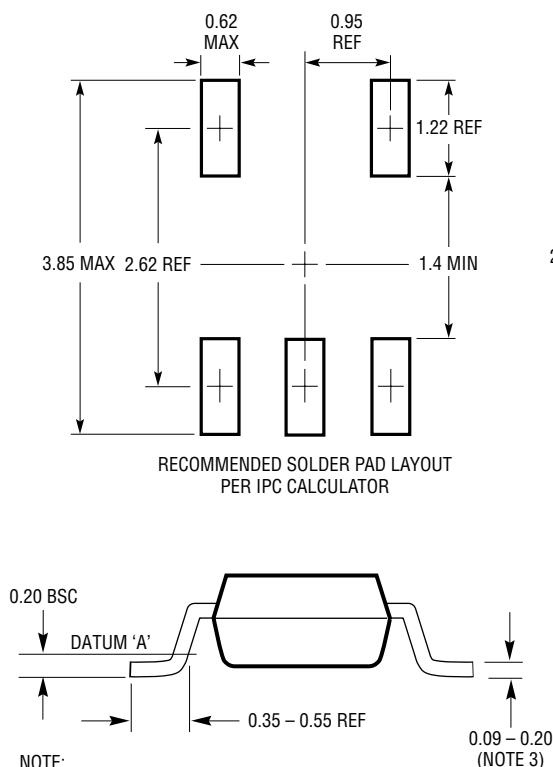
PACKAGE DESCRIPTION

MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)



PACKAGE DESCRIPTION

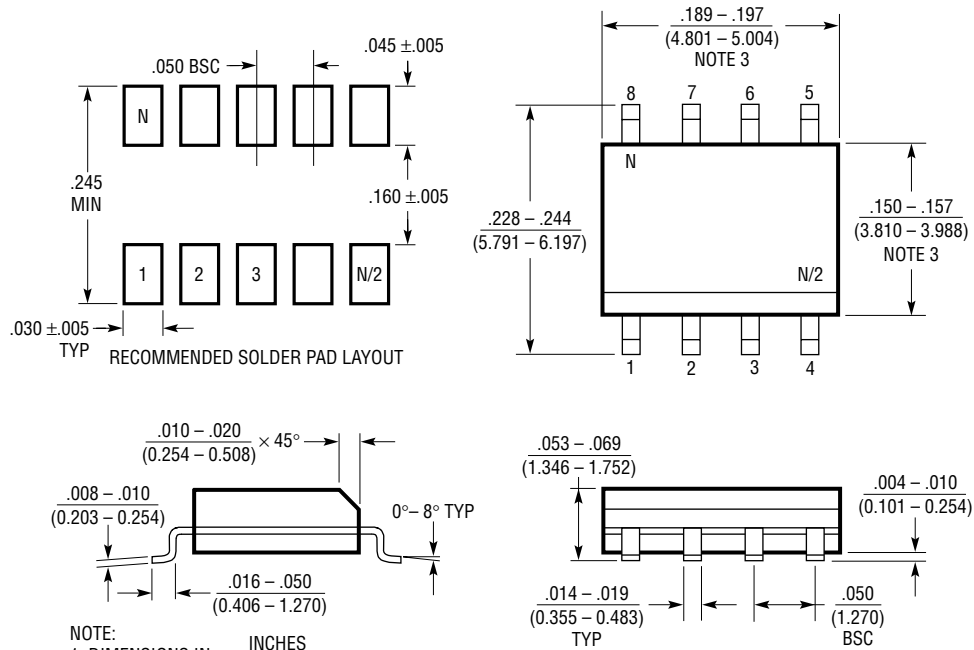
S5 Package 5-Lead Plastic SOT-23 (Reference LTC DWG # 05-08-1633)



ATTENTION: ORIGINAL SOT23-5L PACKAGE.
MOST SOT23-5L PRODUCTS CONVERTED TO THIN SOT23
PACKAGE, DRAWING # 05-08-1635 AFTER APPROXIMATELY
APRIL 2001 SHIP DATE

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

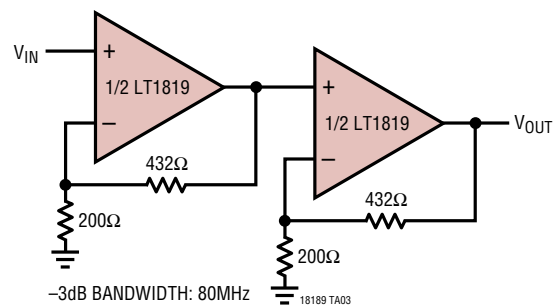


- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

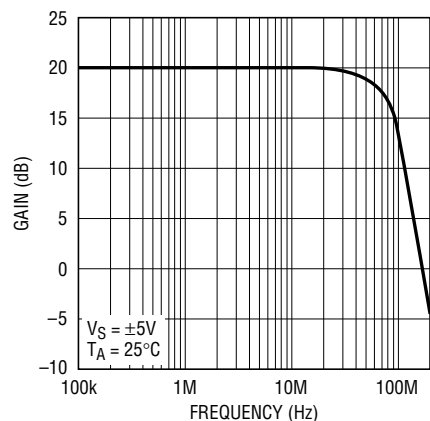
S08 0502

TYPICAL APPLICATION

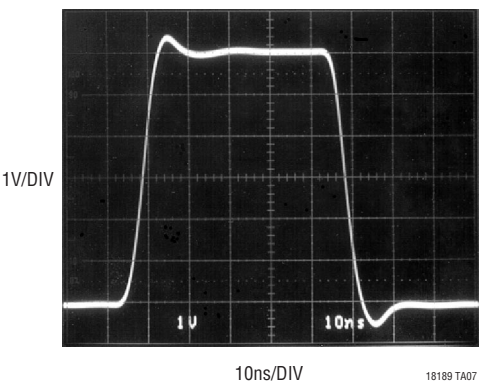
80MHz, 20dB Gain Block



20dB Gain Block Frequency Response



Large-Signal Transient Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current
LT1806/LT1807	Single/Dual 325MHz, 140V/ μ s Rail-to-Rail I/O Op Amps	Low Noise: 3.5nV/ $\sqrt{Hz}$
LT1809/LT1810	Single/Dual 180MHz, 350V/ μ s Rail-to-Rail I/O Op Amps	Low Distortion: -90dBc at 5MHz
LT1812/LT1813/LT1814	Single/Dual/Quad 100MHz, 750V/ μ s Op Amps	Low Power: 3.6mA Max at $\pm 5V$
LT1815/LT1816/LT1817	Single/Dual/Quad 220MHz, 1500V/ μ s Op Amps	Programmable Supply Current
LT6203/LT6204	Dual/Quad 100MHz, Rail-to-Rail I/O Op Amps	1.9nV/ $\sqrt{Hz}$ Noise, 3mA Max