

# 74VHC175 Quad D-Type Flip-Flop

## Features

- High Speed:  $f_{MAX} = 210\text{MHz}$  (Typ.) at  $V_{CC} = 5\text{V}$
- Low power dissipation:  $I_{CC} = 4\mu\text{A}$  (Max.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8\text{V}$  (Max.)
- Pin and function compatible with 74HC175

## General Description

The VHC175 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

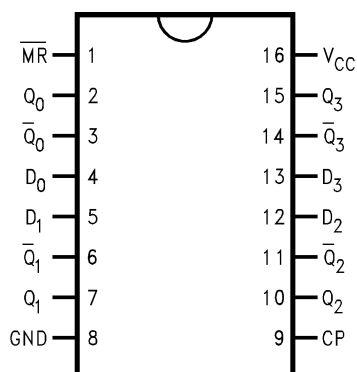
An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

## Ordering Information

| Order Number | Package Number | Package Description                                                          |
|--------------|----------------|------------------------------------------------------------------------------|
| 74VHC175M    | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC175SJ   | M16D           | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide                |
| 74VHC175MTC  | MTC16          | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

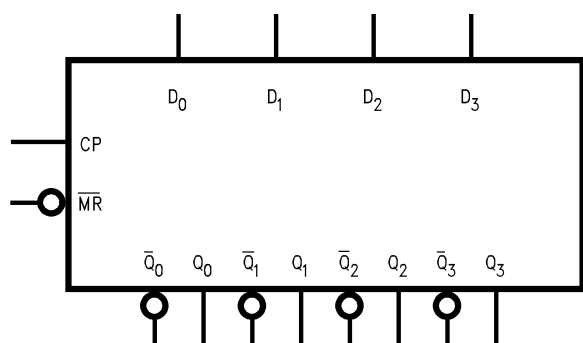
## Connection Diagram



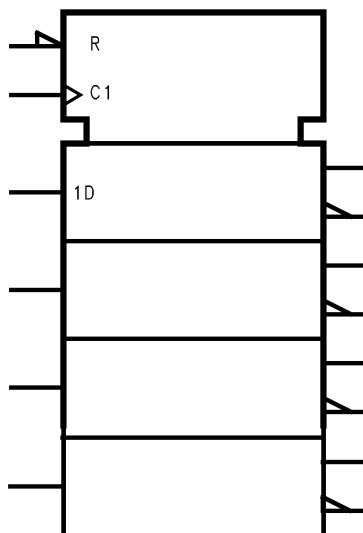
## Pin Description

| Pin Names                       | Description        |
|---------------------------------|--------------------|
| $D_0-D_3$                       | Data Inputs        |
| CP                              | Clock Pulse Input  |
| MR                              | Master Reset Input |
| $Q_0-Q_3$                       | True Outputs       |
| $\overline{Q_0}-\overline{Q_3}$ | Complement Outputs |

## Logic Symbol



IEEE/IEC



## Functional Description

The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## Truth Table

| Inputs @ $t_n$ ,<br>$\overline{MR} = H$ |  | Outputs @ $t_{n+1}$ |             |
|-----------------------------------------|--|---------------------|-------------|
| $D_n$                                   |  | $Q_n$               | $\bar{Q}_n$ |
| L                                       |  | L                   | H           |
| H                                       |  | H                   | L           |

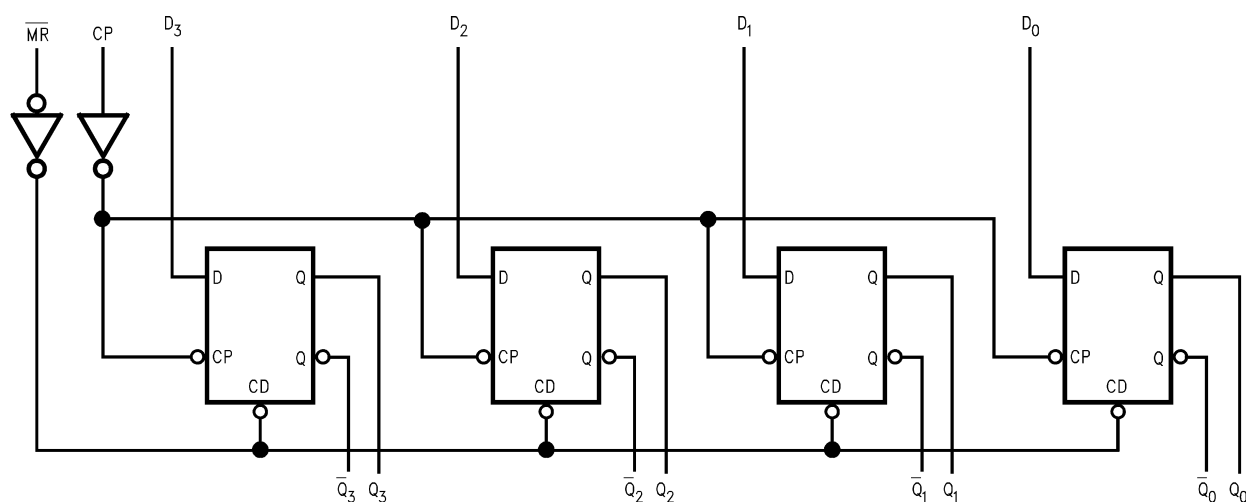
H = HIGH Voltage Level

L = LOW Voltage Level

$t_n$  = Bit Time before Clock Pulse

$t_{n+1}$  = Bit Time after Clock Pulse

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol    | Parameter                                | Rating                   |
|-----------|------------------------------------------|--------------------------|
| $V_{CC}$  | Supply Voltage                           | -0.5V to +7.0V           |
| $V_{IN}$  | DC Input Voltage                         | -0.5V to +7.0V           |
| $V_{OUT}$ | DC Output Voltage                        | -0.5V to $V_{CC} + 0.5V$ |
| $I_{IK}$  | Input Diode Current                      | -20mA                    |
| $I_{OK}$  | Output Diode Current                     | $\pm 20mA$               |
| $I_{OUT}$ | DC Output Current                        | $\pm 25mA$               |
| $I_{CC}$  | DC $V_{CC}$ / GND Current                | $\pm 50mA$               |
| $T_{STG}$ | Storage Temperature                      | -65°C to +150°C          |
| $T_L$     | Lead Temperature (Soldering, 10 seconds) | 260°C                    |

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol     | Parameter                                                                         | Rating                            |
|------------|-----------------------------------------------------------------------------------|-----------------------------------|
| $V_{CC}$   | Supply Voltage                                                                    | 2.0V to +5.5V                     |
| $V_{IN}$   | Input Voltage                                                                     | 0V to +5.5V                       |
| $V_{OUT}$  | Output Voltage                                                                    | 0V to $V_{CC}$                    |
| $T_{OPR}$  | Operating Temperature                                                             | -40°C to +85°C                    |
| $t_r, t_f$ | Input Rise and Fall Time,<br>$V_{CC} = 3.3V \pm 0.3V$<br>$V_{CC} = 5.0V \pm 0.5V$ | 0ns/V ~ 100ns/V<br>0ns/V ~ 20ns/V |

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol   | Parameter                 | $V_{CC}$ (V) | Conditions                       | $T_A = 25^\circ\text{C}$  |      |                     | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ |                     | Units         |
|----------|---------------------------|--------------|----------------------------------|---------------------------|------|---------------------|-------------------------------------------------|---------------------|---------------|
|          |                           |              |                                  | Min.                      | Typ. | Max.                | Min.                                            | Max.                |               |
| $V_{IH}$ | HIGH Level Input Voltage  | 2.0          |                                  | 1.50                      |      |                     | 1.50                                            |                     | V             |
|          |                           | 3.0–5.5      |                                  | $0.7 \times V_{CC}$       |      |                     | $0.7 \times V_{CC}$                             |                     |               |
| $V_{IL}$ | LOW Level Input Voltage   | 2.0          |                                  |                           |      | 0.50                |                                                 | 0.50                | V             |
|          |                           | 3.0–5.5      |                                  |                           |      | $0.3 \times V_{CC}$ |                                                 | $0.3 \times V_{CC}$ |               |
| $V_{OH}$ | HIGH Level Output Voltage | 2.0          | $V_{IN} = V_{IH}$<br>or $V_{IL}$ | $I_{OH} = -50\mu\text{A}$ | 1.9  | 2.0                 |                                                 | 1.9                 | V             |
|          |                           | 3.0          |                                  |                           | 2.9  | 3.0                 |                                                 | 2.9                 |               |
|          |                           | 4.5          |                                  |                           | 4.4  | 4.5                 |                                                 | 4.4                 |               |
|          |                           | 3.0          |                                  | $I_{OH} = -4\text{mA}$    | 2.58 |                     |                                                 | 2.48                |               |
|          |                           | 4.5          |                                  | $I_{OH} = -8\text{mA}$    | 3.94 |                     |                                                 | 3.80                |               |
|          |                           |              |                                  |                           |      |                     |                                                 |                     |               |
| $V_{OL}$ | LOW Level Output Voltage  | 2.0          | $V_{IN} = V_{IH}$<br>or $V_{IL}$ | $I_{OL} = 50\mu\text{A}$  |      | 0.0                 | 0.1                                             |                     | V             |
|          |                           | 3.0          |                                  |                           |      | 0.0                 | 0.1                                             |                     |               |
|          |                           | 4.5          |                                  |                           |      | 0.0                 | 0.1                                             |                     |               |
|          |                           | 3.0          |                                  | $I_{OL} = 4\text{mA}$     |      |                     | 0.36                                            | 0.44                |               |
|          |                           | 4.5          |                                  | $I_{OL} = 8\text{mA}$     |      |                     | 0.36                                            | 0.44                |               |
|          |                           |              |                                  |                           |      |                     |                                                 |                     |               |
| $I_{IN}$ | Input Leakage Current     | 0–5.5        | $V_{IN} = 5.5\text{V or GND}$    |                           |      | $\pm 0.1$           |                                                 | $\pm 1.0$           | $\mu\text{A}$ |
| $I_{CC}$ | Quiescent Supply Current  | 5.5          | $V_{IN} = V_{CC} \text{ or GND}$ |                           |      | 4.0                 |                                                 | 40.0                | $\mu\text{A}$ |

## Noise Characteristics

| Symbol          | Parameter                                | $V_{CC}$ (V) | $T_A = 25^\circ\text{C}$ |        | Units | Conditions          |
|-----------------|------------------------------------------|--------------|--------------------------|--------|-------|---------------------|
|                 |                                          |              | Typ.                     | Limits |       |                     |
| $V_{OLP}^{(2)}$ | Quiet Output Maximum Dynamic $V_{OL}$    | 5.0          | 0.4                      | 0.8    | V     | $C_L = 50\text{pF}$ |
| $V_{OLV}^{(2)}$ | Quiet Output Minimum Dynamic $V_{OL}$    | 5.0          | –0.4                     | –0.8   | V     | $C_L = 50\text{pF}$ |
| $V_{IHD}^{(2)}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0          |                          | 3.5    | V     | $C_L = 50\text{pF}$ |
| $V_{ILD}^{(2)}$ | Maximum LOW Level Dynamic Input Voltage  | 5.0          |                          | 1.5    | V     | $C_L = 50\text{pF}$ |

## Note:

2. Parameter guaranteed by design.

## AC Electrical Characteristics

| Symbol                                | Parameter                                                           | V <sub>CC</sub> (V) | Conditions                           | T <sub>A</sub> = 25°C |      |      | T <sub>A</sub> = -40°C to +85°C |      | Units |
|---------------------------------------|---------------------------------------------------------------------|---------------------|--------------------------------------|-----------------------|------|------|---------------------------------|------|-------|
|                                       |                                                                     |                     |                                      | Min.                  | Typ. | Max. | Min.                            | Max. |       |
| f <sub>MAX</sub>                      | Maximum Clock Frequency                                             | 3.3 ± 0.3           | C <sub>L</sub> = 15pF                | 90                    | 140  |      | 75                              |      | MHz   |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                | 50                    | 75   |      | 45                              |      |       |
|                                       |                                                                     | 5.0 ± 0.5           | C <sub>L</sub> = 15pF                | 150                   | 210  |      | 125                             |      | MHz   |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                | 85                    | 115  |      | 75                              |      |       |
| t <sub>PLH</sub> , t <sub>PHL</sub>   | Propagation Delay Time, (CP to Q <sub>n</sub> or $\overline{Q}_n$ ) | 3.3 ± 0.3           | C <sub>L</sub> = 15pF                |                       | 7.5  | 11.5 | 1.0                             | 13.5 | ns    |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                |                       | 10.0 | 15.0 | 1.0                             | 17.0 |       |
|                                       |                                                                     | 5.0 ± 0.5           | C <sub>L</sub> = 15pF                |                       | 4.8  | 7.3  | 1.0                             | 8.5  | ns    |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                |                       | 6.3  | 9.3  | 1.0                             | 10.5 |       |
| t <sub>PLH</sub> , t <sub>PHL</sub>   | Propagation Delay Time, (MR to Q <sub>n</sub> or $\overline{Q}_n$ ) | 3.3 ± 0.3           | C <sub>L</sub> = 15pF                |                       | 6.3  | 10.1 | 1.0                             | 12.0 | ns    |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                |                       | 8.8  | 13.6 | 1.0                             | 15.5 |       |
|                                       |                                                                     | 5.0 ± 0.5           | C <sub>L</sub> = 15pF                |                       | 4.3  | 6.4  | 1.0                             | 7.5  | ns    |
|                                       |                                                                     |                     | C <sub>L</sub> = 50pF                |                       | 5.8  | 8.4  | 1.0                             | 9.5  |       |
| t <sub>OSLH</sub> , t <sub>OSHL</sub> | Output to Output Skew                                               | 3.3 ± 0.3           | C <sub>L</sub> = 50pF                |                       |      | 1.5  |                                 | 1.5  |       |
|                                       |                                                                     | 5.0 ± 0.5           | C <sub>L</sub> = 50pF <sup>(3)</sup> |                       |      | 1.0  |                                 | 1.0  |       |
| C <sub>IN</sub>                       | Input Capacitance                                                   |                     | V <sub>CC</sub> = Open               |                       | 4    | 10   |                                 | 10   | pF    |
| C <sub>PD</sub>                       | Power Dissipation Capacitance                                       |                     | <sup>(4)</sup>                       |                       | 44   |      |                                 |      | pF    |

## Notes:

3. Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$ ;  $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$ .

4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:

I<sub>CC</sub> (opr.) = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>IN</sub> + I<sub>CC</sub>/4 (per F/F), and the total C<sub>PD</sub> when n pcs of the Flip-Flop operate can be calculated by the following equation: C<sub>PD</sub> (total) = 30 + 14 • n

## AC Operating Requirements

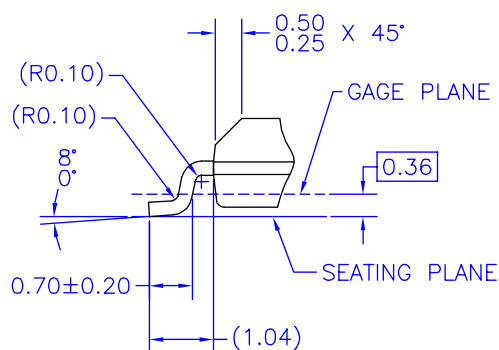
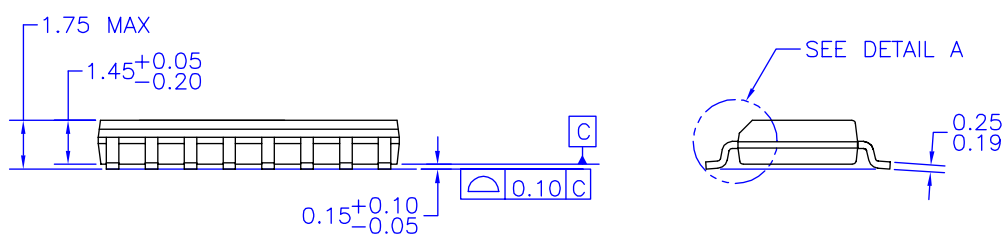
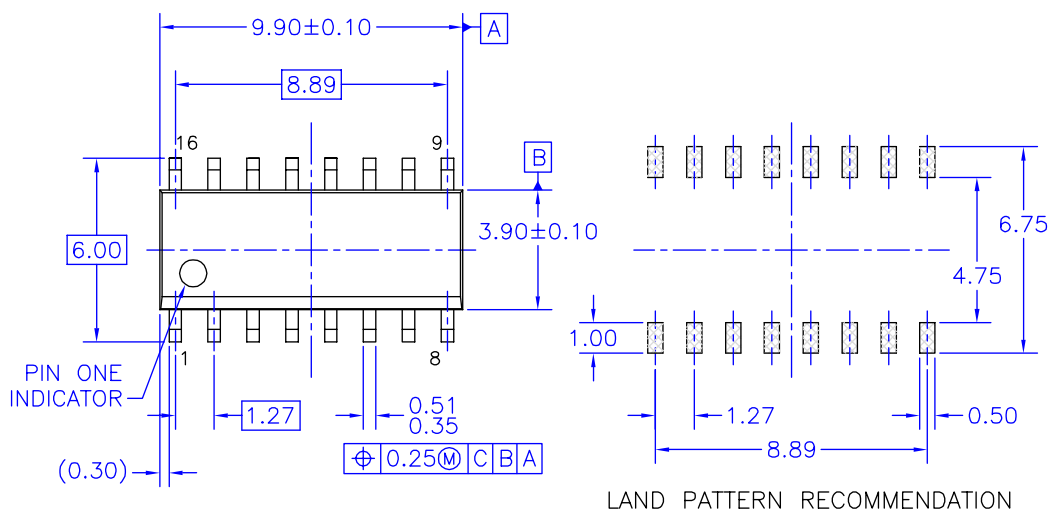
| Symbol                                 | Parameter                                | V <sub>CC</sub> (V) <sup>(5)</sup> | T <sub>A</sub> = 25°C |                    | T <sub>A</sub> = −40°C to +85°C | Units |
|----------------------------------------|------------------------------------------|------------------------------------|-----------------------|--------------------|---------------------------------|-------|
|                                        |                                          |                                    | Typ.                  | Guaranteed Minimum |                                 |       |
| t <sub>W</sub> (L), t <sub>W</sub> (H) | Minimum Pulse Width (CP)                 | 3.3                                |                       | 5.0                | 5.0                             | ns    |
|                                        |                                          | 5.0                                |                       | 5.0                | 5.0                             |       |
| t <sub>W</sub> (L)                     | Minimum Pulse Width ( $\overline{MR}$ )  | 3.3                                |                       | 5.0                | 5.0                             | ns    |
|                                        |                                          | 5.0                                |                       | 5.0                | 5.0                             |       |
| t <sub>S</sub>                         | Minimum Setup Time (Dn to CP)            | 3.3                                |                       | 5.0                | 5.0                             | ns    |
|                                        |                                          | 5.0                                |                       | 4.0                | 4.0                             |       |
| t <sub>H</sub>                         | Minimum Hold Time (Dn to CP)             | 3.3                                |                       | 1.0                | 1.0                             | ns    |
|                                        |                                          | 5.0                                |                       | 1.0                | 1.0                             |       |
| t <sub>REC</sub>                       | Minimum Removal Time ( $\overline{MR}$ ) | 3.3                                |                       | 5.0                | 5.0                             | ns    |
|                                        |                                          | 5.0                                |                       | 5.0                | 5.0                             |       |

## Note:

5. V<sub>CC</sub> is 3.3 ± 0.3V or 5.0 ± 0.5V

## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

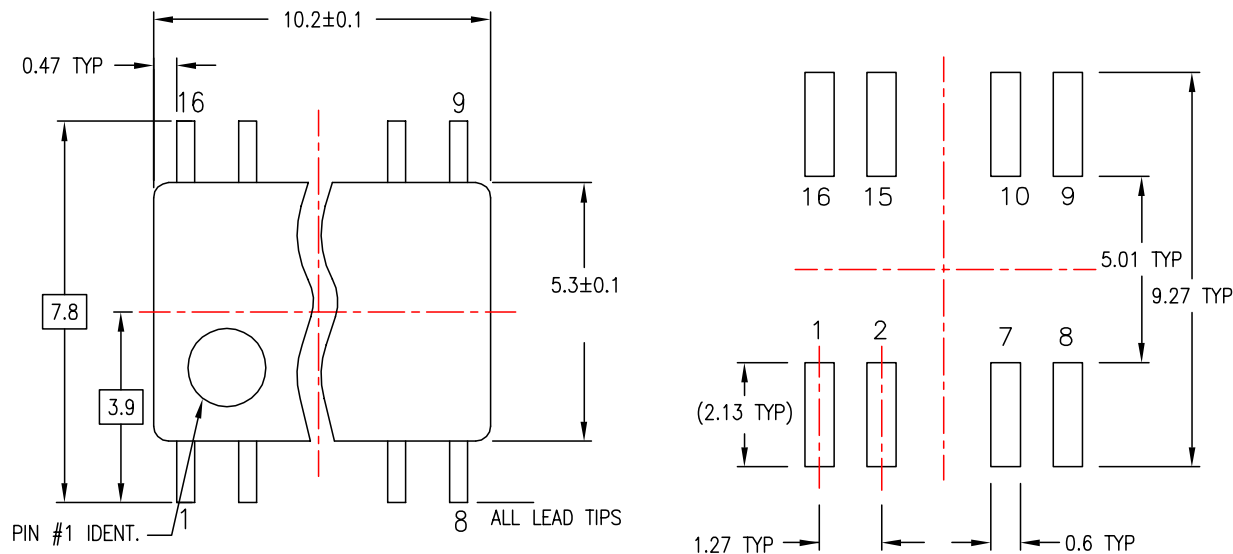
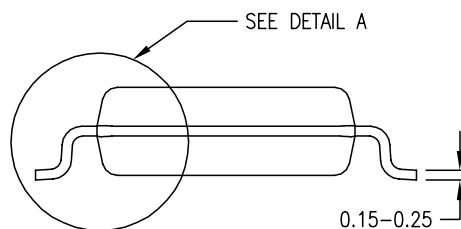
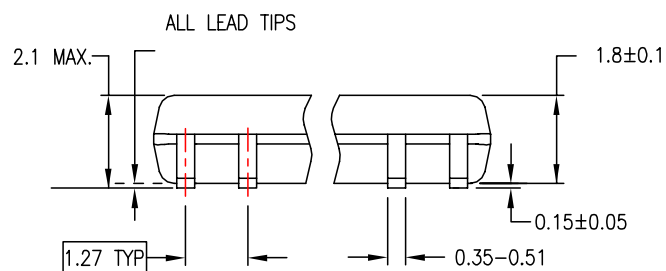
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICROINCHES / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

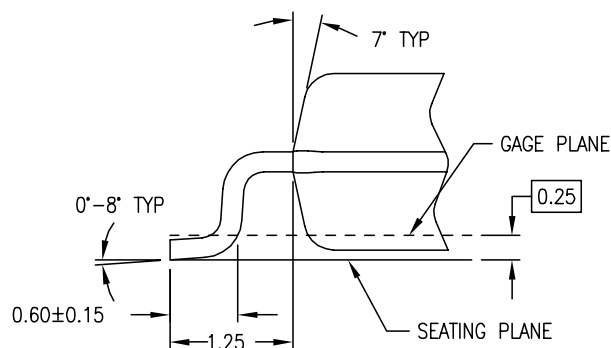
**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.

LAND PATTERN RECOMMENDATIONDIMENSIONS ARE IN MILLIMETERS

## NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

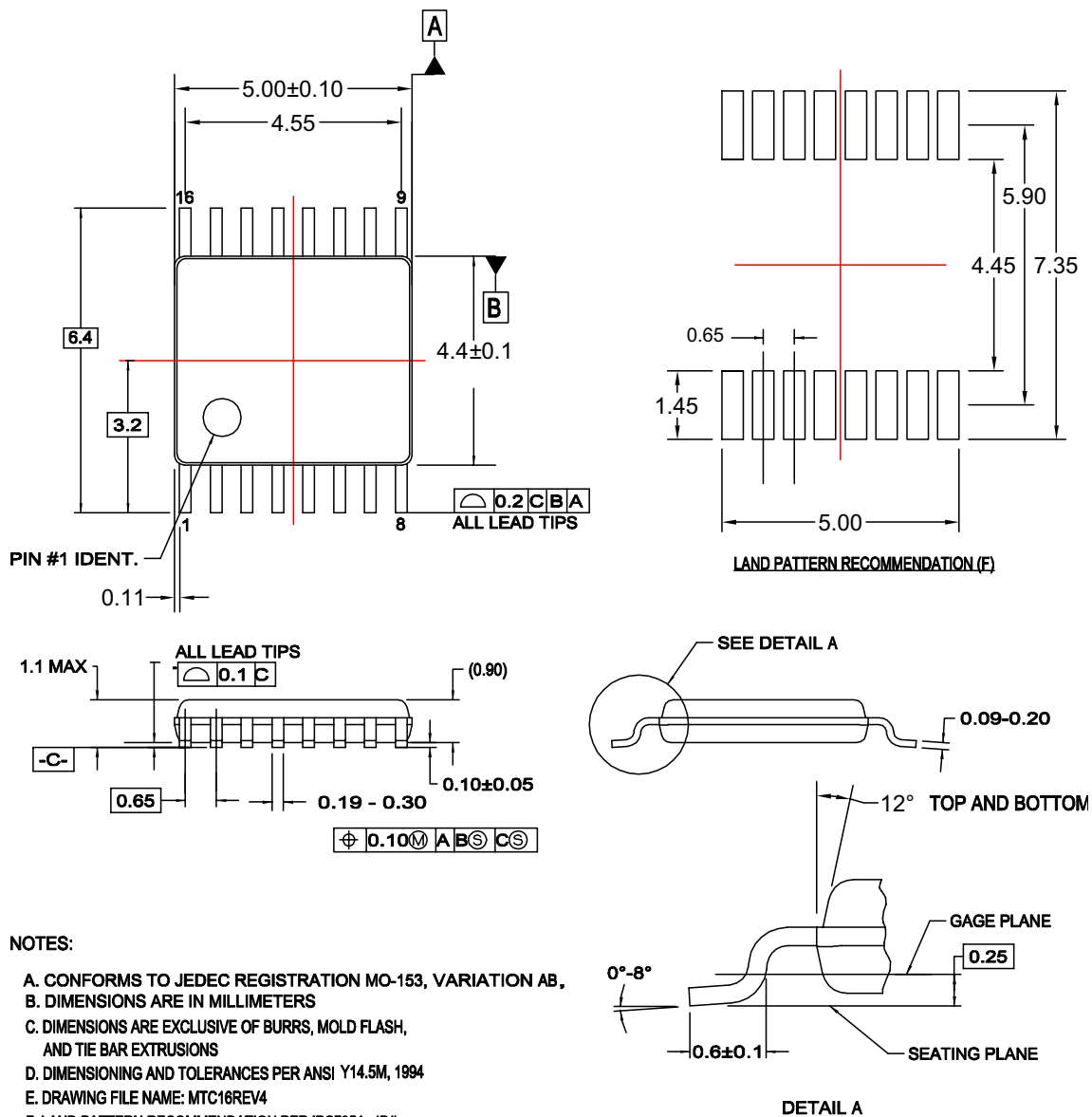
DETAIL A

M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M16D**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



MTC16rev4

**Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16**





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| ActiveArray <sup>™</sup>                         | IntelliMAX <sup>™</sup>        | Programmable Active Droop <sup>™</sup>                                            | TinyLogic <sup>®</sup>      |
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| Build it Now <sup>™</sup>                        | MICROCOUPLER <sup>™</sup>      | QS <sup>™</sup>                                                                   | TinyPower <sup>™</sup>      |
| CoolFET <sup>™</sup>                             | MicroPak <sup>™</sup>          | QT Optoelectronics <sup>™</sup>                                                   | TinyWire <sup>™</sup>       |
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| E <sup>2</sup> CMOS <sup>™</sup>                 | OCX <sup>™</sup>               | SMART START <sup>™</sup>                                                          | VCX <sup>™</sup>            |
| EcoSPARK <sup>®</sup>                            | OCXPro <sup>™</sup>            | SPM <sup>®</sup>                                                                  | Wire <sup>™</sup>           |
| EnSigna <sup>™</sup>                             | OPTOLOGIC <sup>®</sup>         | STEALTH <sup>™</sup>                                                              |                             |
| FACT Quiet Series <sup>™</sup>                   | OPTOPLANAR <sup>®</sup>        | SuperFET <sup>™</sup>                                                             |                             |
| FACT <sup>®</sup>                                | PACMAN <sup>™</sup>            | SuperSOT <sup>™</sup> -3                                                          |                             |
| FAST <sup>®</sup>                                | PDP-SPM <sup>™</sup>           | SuperSOT <sup>™</sup> -6                                                          |                             |
| FASTr <sup>™</sup>                               | POP <sup>™</sup>               | SuperSOT <sup>™</sup> -8                                                          |                             |
| FPS <sup>™</sup>                                 | Power220 <sup>®</sup>          | SyncFET <sup>™</sup>                                                              |                             |
| FRFET <sup>®</sup>                               | Power247 <sup>®</sup>          | TCM <sup>™</sup>                                                                  |                             |
| GlobalOptoisolator <sup>™</sup>                  | PowerEdge <sup>™</sup>         | The Power Franchise <sup>®</sup>                                                  |                             |
| GTO <sup>™</sup>                                 | PowerSaver <sup>™</sup>        |  |                             |
| HiSeC <sup>™</sup>                               |                                |                                                                                   |                             |

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status         | Definition                                                                                                                                                                                               |
|--------------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information      | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.                                                                       |
| Preliminary              | First Production       | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production        | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.                                                   |
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