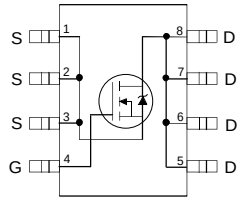
International
IOR Rectifier

IRF7413ZPbF

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	I_D
30V	10mΩ@V_{GS} = 10V	13A



Top View


SO-8

Applications

- Control FET for Notebook Processor Power
- Control and Synchronous Rectifier MOSFET for Graphics Cards and POL Converters in Computing, Networking and Telecommunication Systems

Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current
- 100% Tested for R_G
- Lead-Free

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	13	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	10	
I_{DM}	Pulsed Drain Current ①	100	
P_D @T_A = 25°C	Power Dissipation	2.5	W
P_D @T_A = 70°C	Power Dissipation	1.6	
	Linear Derating Factor	0.02	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	–––	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	–––	50	

Notes ① through ④ are on page 10

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.025	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	8.0	10	mΩ	V_{GS} = 10V, I_D = 13A ③
		—	10.5	13		V_{GS} = 4.5V, I_D = 10A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.0	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	62	—	—	S	V_{DS} = 15V, I_D = 10A
Q_g	Total Gate Charge	—	9.5	14		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	3.0	—		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.0	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	3.0	—		I_D = 10A
Q_{godr}	Gate Charge Overdrive	—	2.5	—		See Fig. 16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	4.0	—		
Q_{oss}	Output Charge	—	5.6	—	nC	V_{DS} = 15V, V_{GS} = 0V
R_G	Gate Resistance	—	2.3	4.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—		V_{DD} = 16V, V_{GS} = 4.5V
t_r	Rise Time	—	6.3	—		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	—	11	—	ns	Clamped Inductive Load
t_f	Fall Time	—	3.8	—		
C_{iss}	Input Capacitance	—	1210	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	270	—	pF	V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	—	140	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	32	mJ
I_{AR}	Avalanche Current ①	—	10	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	100		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	24	36	ns	T_J = 25°C, I_F = 10A, V_{DD} = 15V
Q_{rr}	Reverse Recovery Charge	—	16	24	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

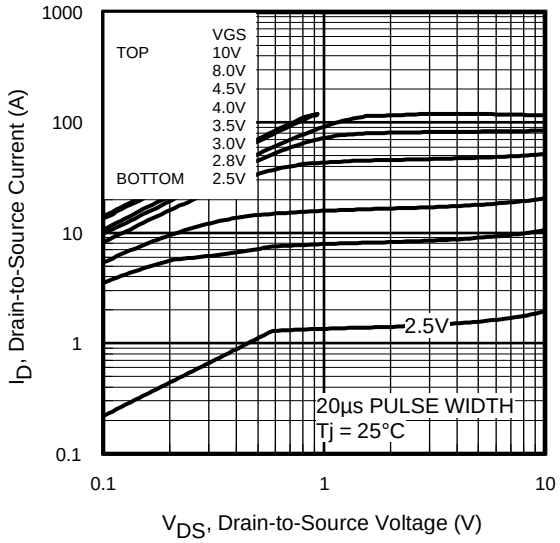


Fig 1. Typical Output Characteristics

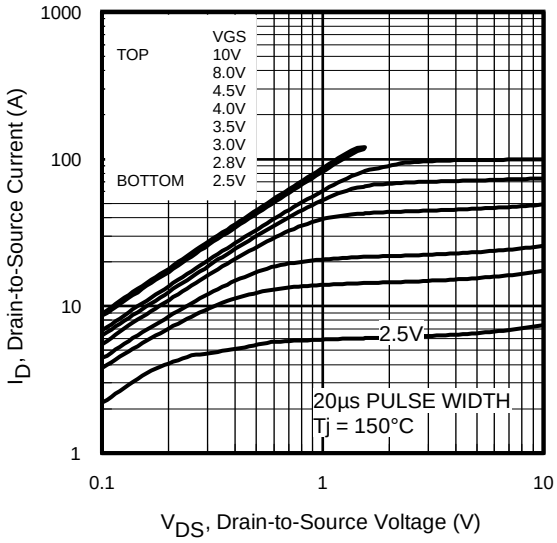


Fig 2. Typical Output Characteristics

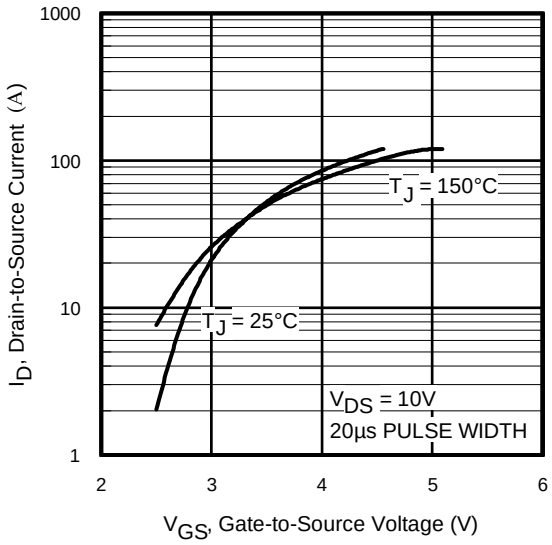


Fig 3. Typical Transfer Characteristics

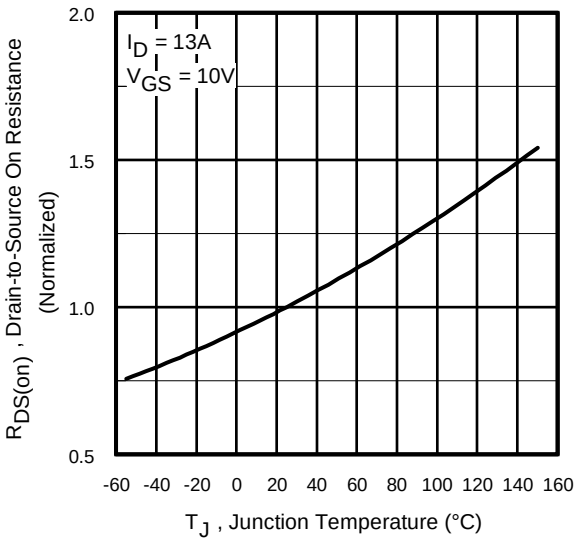


Fig 4. Normalized On-Resistance vs. Temperature

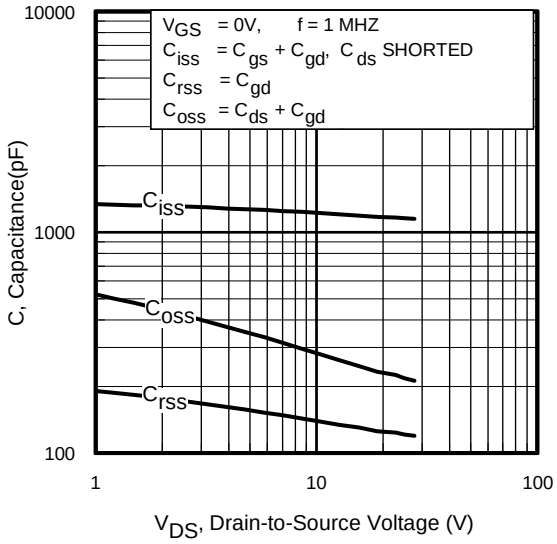


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

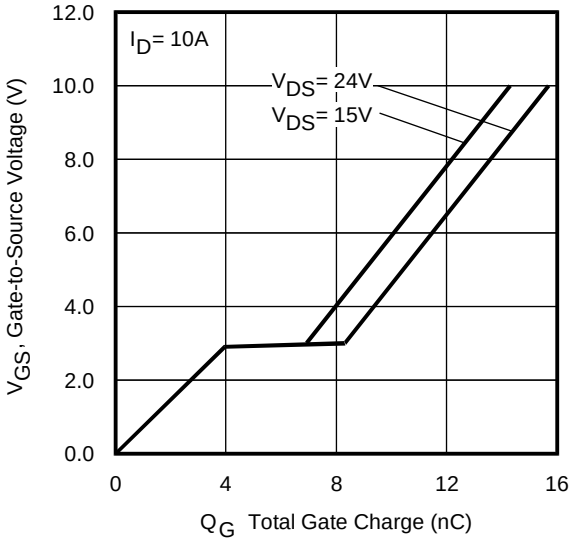


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

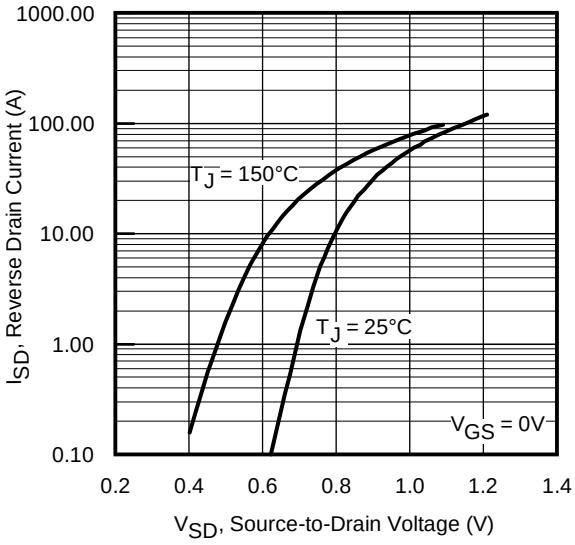


Fig 7. Typical Source-Drain Diode Forward Voltage

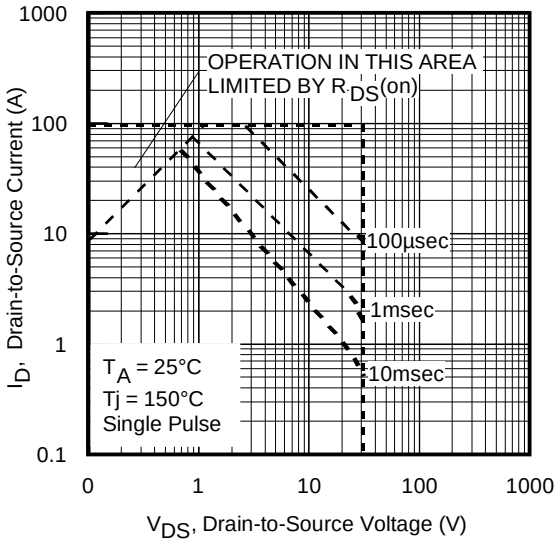


Fig 8. Maximum Safe Operating Area

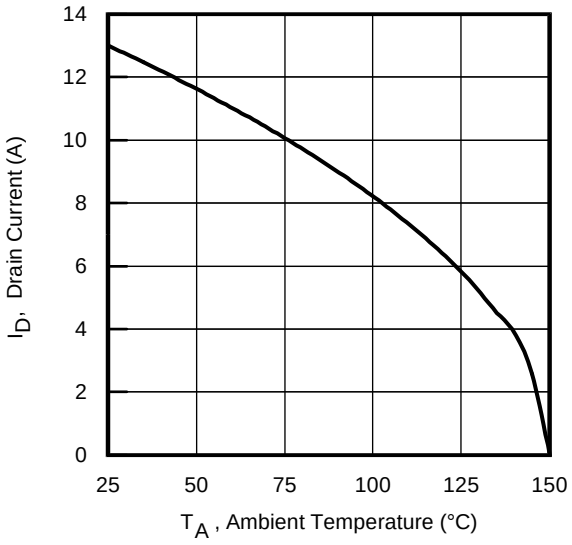


Fig 9. Maximum Drain Current vs. Ambient Temperature

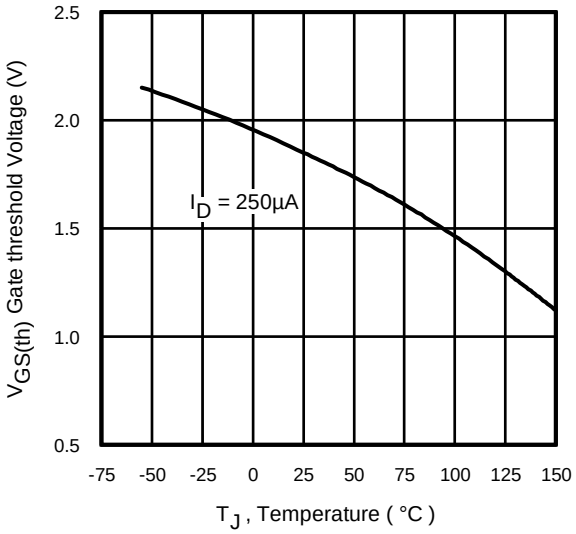


Fig 10. Threshold Voltage vs. Temperature

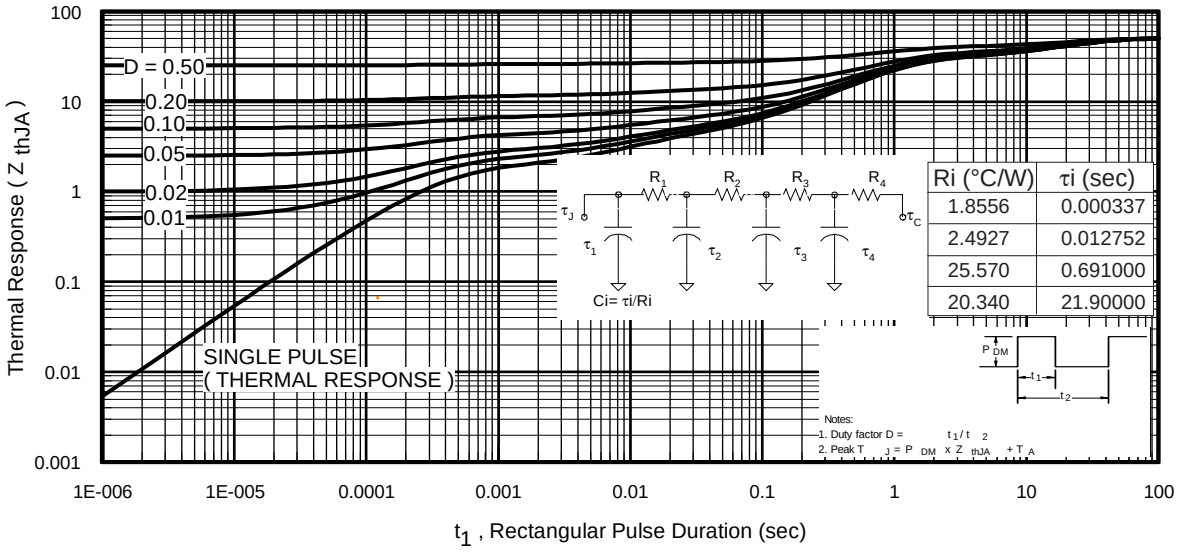


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

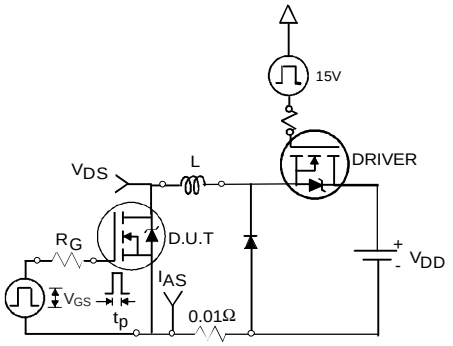


Fig 12a. Unclamped Inductive Test Circuit

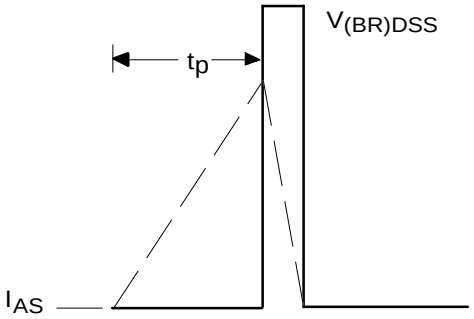


Fig 12b. Unclamped Inductive Waveforms

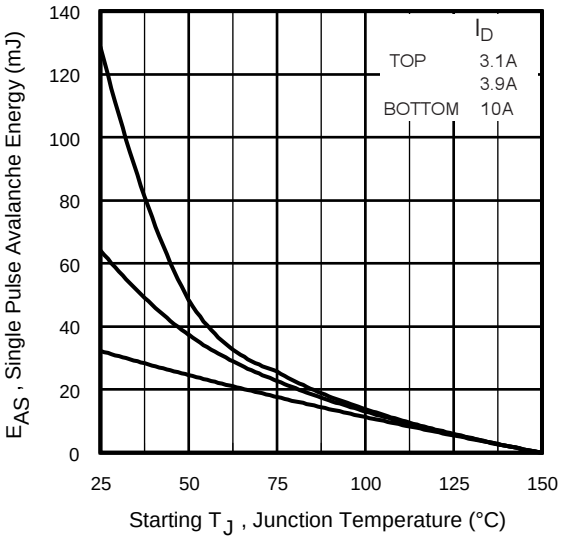


Fig 12c. Maximum Avalanche Energy vs. Drain Current

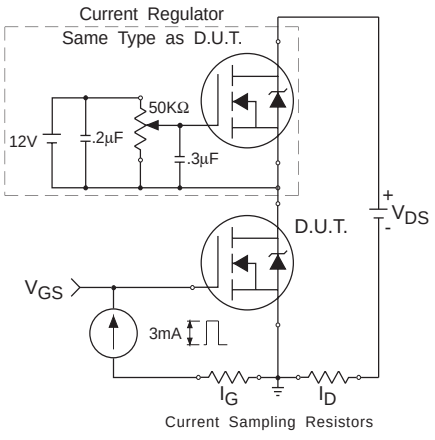


Fig 13. Gate Charge Test Circuit

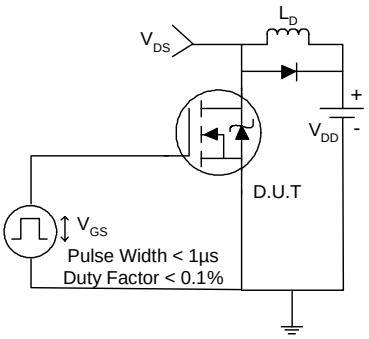


Fig 14a. Switching Time Test Circuit

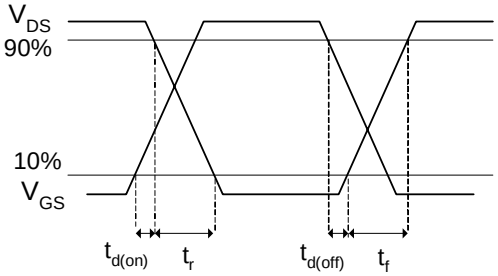


Fig 14b. Switching Time Waveforms

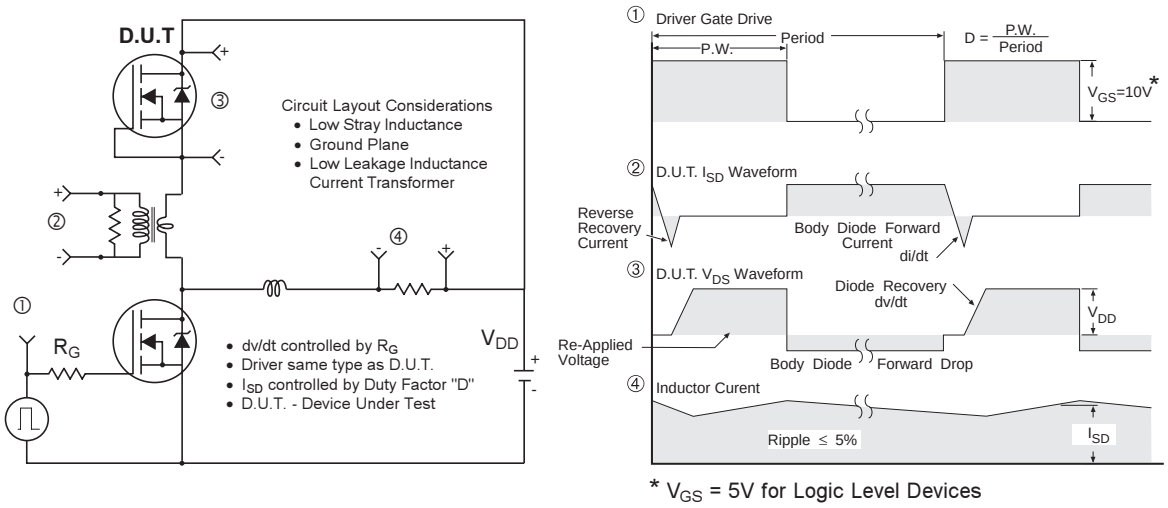


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

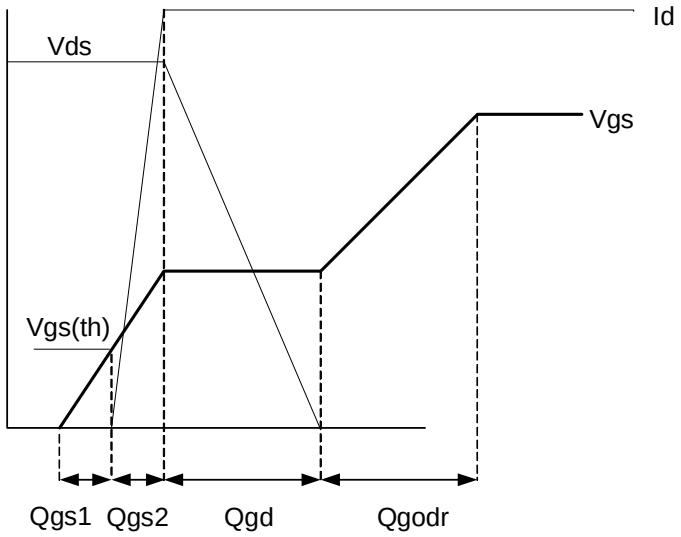


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^*_{output}$$

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

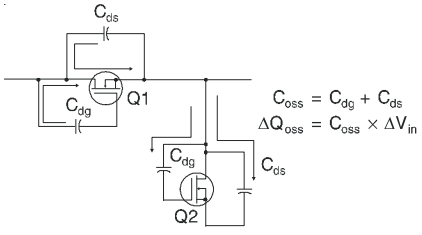
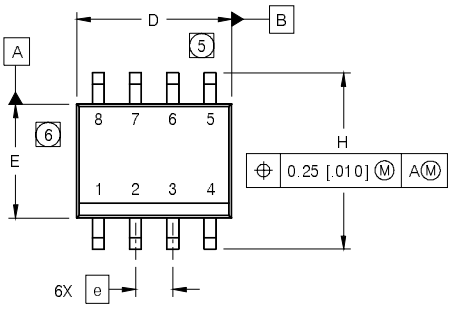
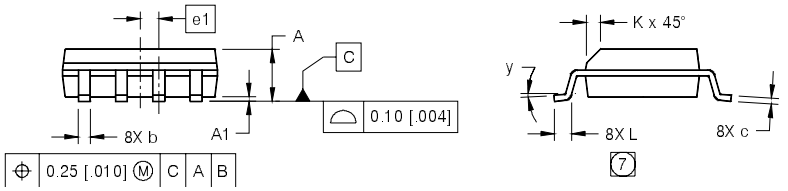


Figure A: Q_{oss} Characteristic

SO-8 Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



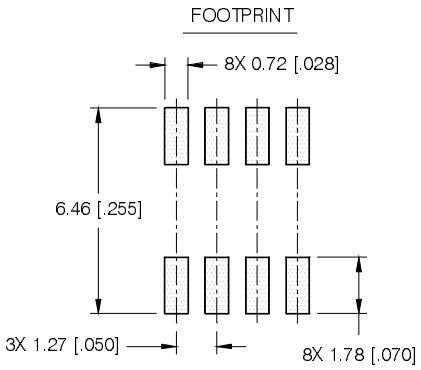
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

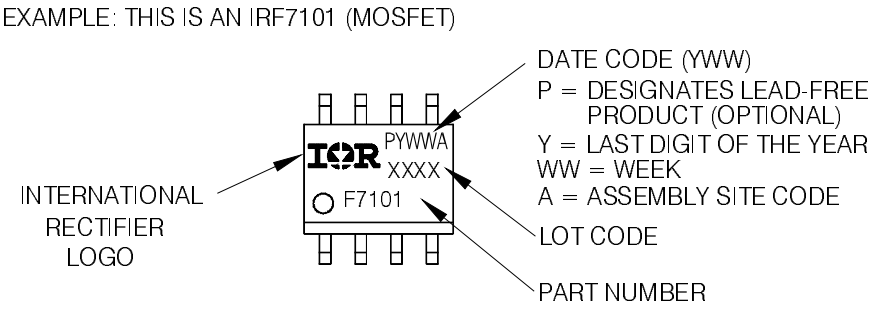
(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

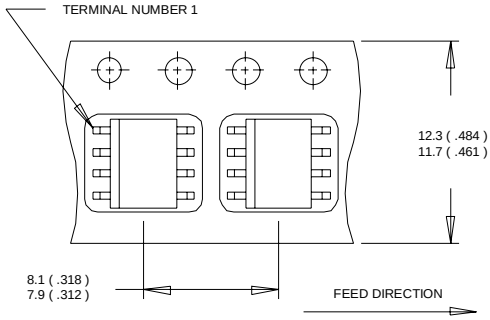


SO-8 Part Marking

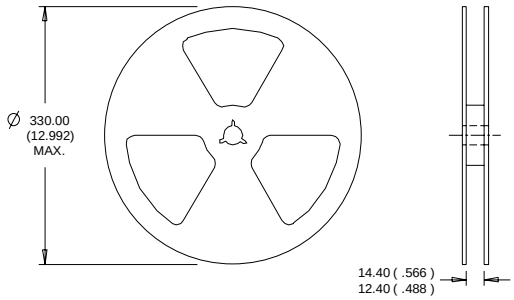


SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.62mH, R_G = 25Ω, I_{AS} = 10A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 06/2006

International
IOR Rectifier

SOIC-8L
Lead Free and RoHS Compliance Document

Contents:

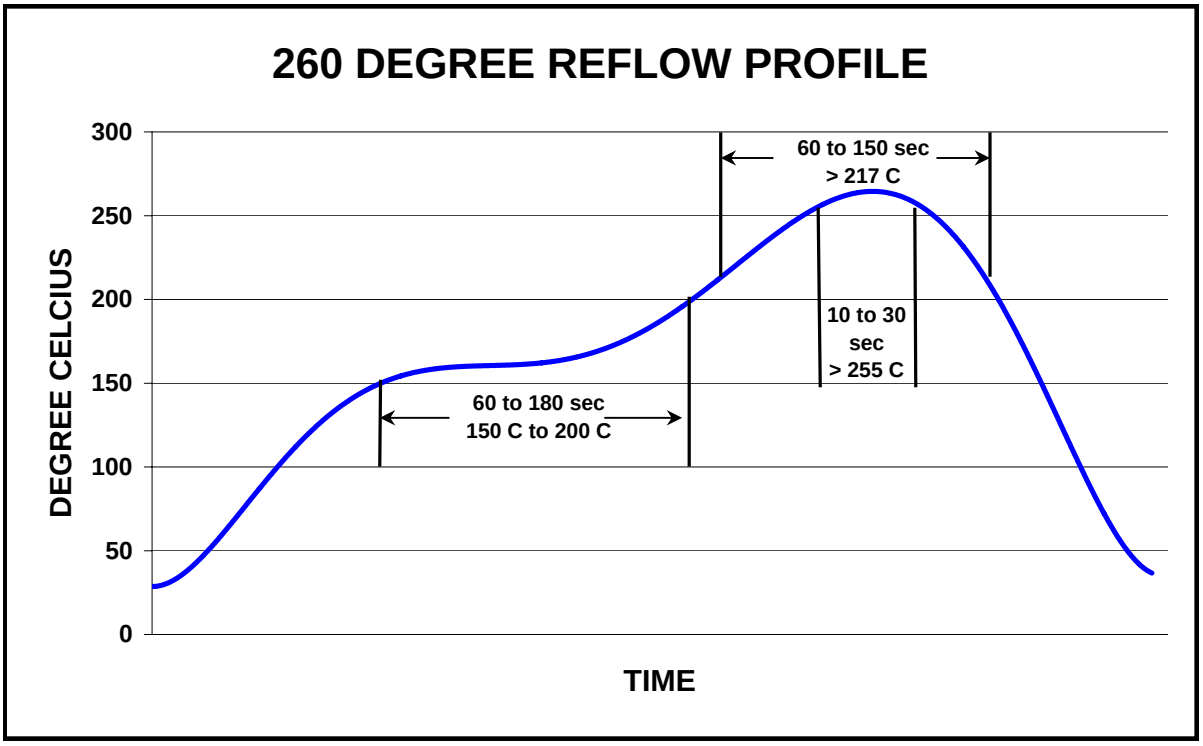
International
IOR Rectifier

SOIC-8L

Component	Material Name	Material Mass (gr/ea)	Element Name Composition	Substance Mass (per device) g	Material Analysis Weight (%)	% of Total Weight
Chip	Silicon	0.00262	Si	0.00262	100%	3.2%
Encapsulant	Epoxy Resin	0.05006	SiO2	0.03550	71%	44.0%
			Epoxy	0.00888	18%	11.0%
			Other	0.00568	11%	7.0%
Lead Frame	Copper	0.02426	Cu	0.02363	97%	29.3%
			Other	0.00063	3%	0.8%
Die Attach	Silver Epoxy	0.00193	Epoxy	0.00017	9%	0.2%
			Ag	0.00088	46%	1.1%
			Aromatic Amine	0.00088	46%	1.1%
Wire bond	Gold	0.00030	Au	0.00030	100%	0.4%
Lead Finish	Tin / Lead	0.00146	Sn	0.00146	100%	1.8%

MSL2 at 260 C

Total Weight (g) **0.08063**



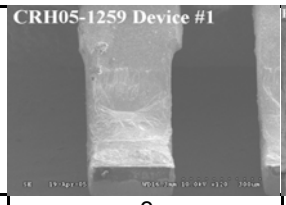
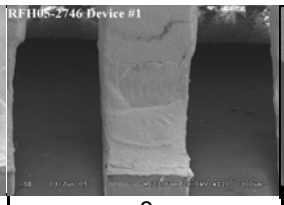
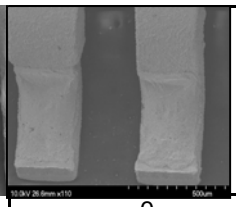
This part is compliant with EU Directive 2002/95/EC (RoHS) and does not contain lead, mercury, cadmium (0.01%), hexavalent chromium, PBB or PBDE in concentrations greater than 0.1%, except as permitted by Annex (7).

Inter
IOR Rectifier

SOIC-8L Tin Whisker Report

Objective: The purpose is to evaluate the Tin whisker growth for various test conditions on PbF products

Part No: IRF7530
Package Type: Micro-8 Micro-8 used for SOIC-8L

Test	Room Temperature Storage	Temperature Humidity Unbias	Temperature Cycling
Test Conditions	30+/-2°C, 60+/-3%RH	60+/-5°C, 87+3/-2%RH	-55 to 85°C
Test Status/Readpoint	NWF	NWF	NWF
Examples:			
			
Whisker Length (μm)	0	0	0

Abbreviation	NWF	WFA	WFO
Whisker length pass/fail criterion	No Whiskers Found Whisker length less than 10 um is considered insignificant	Whiskers found within acceptable range Whisker length less than 40 um is considered pass	Whiskers found over acceptable range Whisker length exceeding 40 um is considered fail

Sn Plating descriptions:

Plating thickness (μin): >300
Annealing conditions: 150°C for 1 hour
Plating finish: 100% Sn Matte

Sample size: 3 pieces per test
Reflow: 1X @ 255°C

International
IOR Rectifier

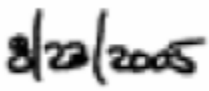
International Rectifier components and their homogeneous sub-components manufactured under the Lead Free Program [1] are in compliance with European Union Directive 2002/95/EC (RoHS Directive) of the European Parliament and of the Council of 27 January 2003. IR parts that have been identified as RoHS compliant do not exceed the maximum limit for following 6 designated substances.

Substance	**Maximum Limit (ppm)**
Cadmium (Cd)	100
Lead (Pb)	1000 [2]
Mercury (Hg)	1000
Hexavalent Chromium (Cr^{6+})	1000
Poly Brominated Biphenyls (PBB)	1000
Poly Brominated Diphenyl Ethers (PBDE)	1000

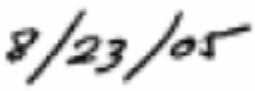
(1) Part numbers typically contain a "PBF" suffix
(2) Maximum limit (ppm) does not apply to applications for which exemptions have been granted by the RoHS Directive

Our statements in this letter regarding RoHS compliance and lead content do not extend to, or apply to any product subjected to unintended contamination, misuse, neglect, accident, improper installation, or to use in violation of instructions furnished by IR. We additionally note that IR products in certain specific large outline packages could contain high temperature solder die attach material having greater than 85% lead content, which is considered exempt from ELV Directive, Article 4(2)(a) by Annex II and RoHS Directive, Article 4(1) by Annex (7).

Authorized signatures for International Rectifier:

Name:  Greg Takagi Date: 

Position: Director, Global Environmental Health and Safety

Name:  Danny Narabal Date: 

Position: Director, Package Engineering

The information contained in this letter is being provided for informational purposes only and to clarify certain information concerning IR products. Nothing provided in this letter is (i) a representation, warranty or agreement to indemnification by IR, (ii) a statement which may form the basis of reliance by IR, (iii) a modification of any of the terms and conditions of sale agreed to in writing between IR and its customers with respect to any IR products, whether previously sold or to be sold in the future.

International
IOR Rectifier

Report Date: 14-Jul-2005
Work Order: 05-03284-01

ELEMENTAL CONTAMINATION TEST RESULTS

Testing performed by: BALAZS ANALYTICAL SERVICES, RWTUV USA INC. ISO 9001:2000 QMS

Air Liquide - Balazs Analytical Services
46409 Landing Parkway, Fremont CA 94538
Telephone (510) 657-0600 Fax (510) 657-2292
Web http://www.balazs.com

Analysis Technique:
Analysis was performed on twelve (12) IC samples to determine the amount of elemental contamination (Cd, Pb, Hg, and As), PVC and PVC blends, asbestos, hexavalent chromium, and organic bromide compounds present in the samples.

Analysis Technique:
Each sample set was ground to pass a 200 mesh screen. Individual samples were analyzed in accordance with the document labeled **"Plastics - Determination of cadmium - Wet decomposition method"**, EN1122, ICS 83.080.01, Method "A". Individual were weighed to +0.01 mg. followed by analysis using ISO 3613: 2000(E), "Chromate Conversion Coatings on Zinc, Cadmium, Aluminum-Zinc Alloys and Zinc-Aluminum alloys---Test Methods." Each sample set was ground to pass a 200 mesh screen. Individual samples were analyzed in accordance with the document labeled "Interim Method for the Determination of Asbestos in Bulk Insulation Samples", EPA-600/M4-82-020, Dec. 1982. Samples were measured utilizing a Leica DMLM compound binocular microscope.
Each sample set was prepared for reflectance mode FTIR utilizing a BioRad FTS6000 FTIR system coupled to a UMA 500 FTIR microscope. The FTIR spectra for reference areas were collected on adjacent clear areas of a control wafer. Infrared spectra were then collected at 8 cm-1 resolution with 1024 scans co-added together prior to Fourier Transformation.
Individual samples were analyzed in accordance with EPA-600 Method 1614 draft method, in conjunction with the appropriate preparation technique.

Elemental Results:

	As	Cd	Hg	Pb
Sample Name	ppm (wt.)	ppm (wt.)	ppm (wt.)	ppm (wt.)
Blank	<1.0	<1.0	<1.0	<1.0
IRF4905PBF (TO-220)	<1.0	<1.0	<1.0	4.1
IRFP450PBF (TO-247)	<1.0	<1.0	<1.0	11.6
IRF740SPBF (D2-PAK)	<1.0	<1.0	<1.0	14600
IRFR3707ZPBF (D-PAK)	<1.0	<1.0	<1.0	4864
IRLL2705PBF (SOT-223)	<1.0	<1.0	<1.0	11100
IRF6603 (DirectFET)	<1.0	<1.0	<1.0	19.2
IRLML6401TRPBF (Micro-3)	<1.0	<1.0	<1.0	6.4
IRLMS6802TRPBF (Micro-6)	<1.0	<1.0	<1.0	9.5
IRF7821PBF(SO-8)	<1.0	<1.0	<1.0	7.6
IR2153PBF (8L PDIP)	<1.0	<1.0	<1.0	9.4
IRF7503TRPBF (Micro-8)	<1.0	<1.0	<1.0	15.8
IR3086AMPBF (20L MLPQ)	<1.0	<1.0	<1.0	8.9

The re-analysis of the IRF740SPBF, IRFR3707ZPBF, IRLL2705PBF indicate that the high Pb is coming from a single internal layer and is exempt per the specifications

International
IOR Rectifier

Results:

	PBB/PDBE	Cr(VI)	PVC	Asbestos
Sample Name	ppm (wt.)	ppm (wt.)	ppm (wt.)	P/NP
Blank	<10.	<1.0	<1.0	NP
IRF4905PBF (TO-220)	<10.	<1.0	<1.0	NP
IRFP450PBF (TO-247)	<10.	<1.0	<1.0	NP
IRF740SPBF (D2-PAK)	<10.	<1.0	<1.0	NP
IRFR3707ZPBF (D-PAK)	<10.	<1.0	<1.0	NP
IRLL2705PBF (SOT-223)	<10.	<1.0	<1.0	NP
IRF6603 (DirectFET)	<10.	<1.0	<1.0	NP
IRLML6401TRPBF (Micro-3)	<10.	<1.0	<1.0	NP
IRLMS6802TRPBF (Micro-6)	<10.	<1.0	<1.0	NP
IRF7821PBF(SO-8)	<10.	<1.0	<1.0	NP
IR2153PBF (8L PDIP)	<10.	<1.0	<1.0	NP
IRF7503TRPBF (Micro-8)	<10.	<1.0	<1.0	NP
IR3086AMPBF (20L MLPQ)	<10.	<1.0	<1.0	NP