171020601/WPMDH1200601J

MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

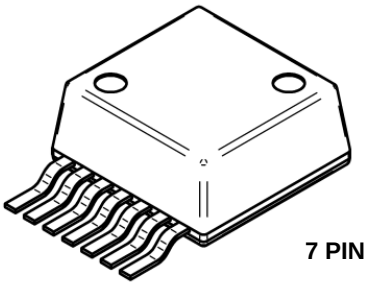
DESCRIPTION

The VDRM series of the MagI³C Power Modules Family comprise a fully integrated current mode DC/DC power supply with both the switching power stage, control circuitry and passive all in one package These devices also feature built-in compensation circuitry and a soft-start feature for a smooth, safe power up. The 7 PIN PFM is an industrial high power density package with a low profile and a small outline.

The VDRM series offers high efficiency and delivers up to 2A of output current with accurate regulated output voltages. It operates from input voltage 6V to 42V.

They are available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The VDRM regulators also have on-board protection circuitry to guard against thermal and electrical damage. Thermal shut-down, over-current, overvoltage and under-voltage protections safeguard the regulator and include a short-circuit protection.



7 PIN PFM

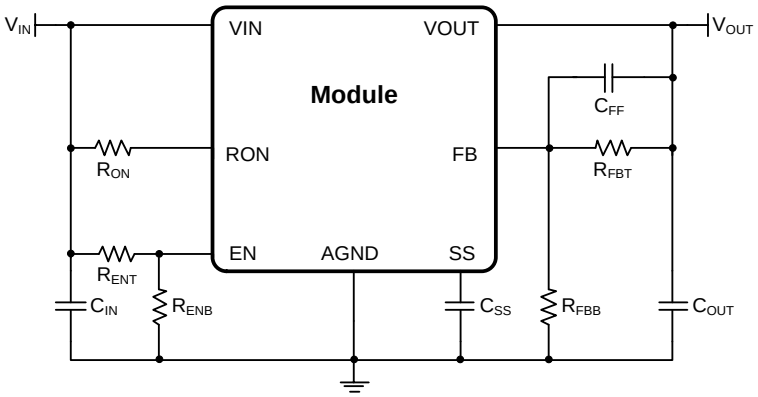
FEATURES

- Peak efficiency up to 90%
- Current capability up to 2A
- Wide input voltage range: 6V-42V
- Wide output voltage range: 0.8V-6V
- Integrated inductor solution for quick time to market and ease of use
- Single exposed pad for best-in-class thermal performance
- Low output voltage ripple
- Under voltage lockout Protection (UVLO)
- Programmable soft-start and frequency
- Thermal shut down, inrush current and output short current protection
- Temperature range: -40 to 125°C
- RoHS & REACh compliant

APPLICATIONS

- Point of Load DC-DC applications
- Servers, Data and Telecom
- System power supplies
- DSPs, FPGAs, MCUs and MPUs
- I/O interface

TYPICAL APPLICATION



PRELIMINARY

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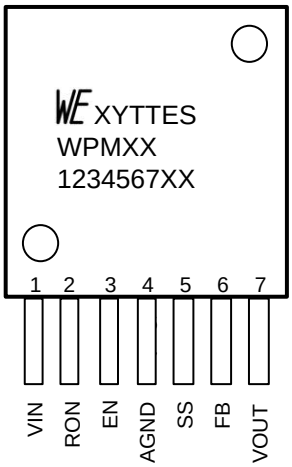
A PACKAGE MARKING



First row: Logo & Date code

Second row: Product family and type

Third row: Parameter code

Top View 7 PIN PFM

B PIN DESCRIPTION

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{IN}	Input power supply
2	R_{ON}	Set the frequency of the application
3	EN	Remote ON/OFF
4	AGND	Reference ground of the device
5	SS	Set up the soft-start function
6	FB	Set up the output voltage
7	V_{OUT}	Regulated output voltage
EP	EP	Exposed Pad - Must be electrically connected to pin 4 external to package

C ORDERING INFORMATION

ORDER CODE	PART ESCRIPTION	PACKAGE	PACKING UNIT
171020601	WPMDH1200601JT	7 PIN PFM	Tape and Reel with 250 Units
178020601	WPMDH1200601JEV	Demokit	evaluation board 1 Unit

D SALES INFORMATION

SALES CONTACTS

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
powermodules@we-online.com

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E ABSOLUTE MAXIMUM RATINGS (1)

Preventive Caution: Exceeding the listed absolute maximum ratings below may affect the device negatively and may cause permanent damage. Therefore operating ratings are conditions under which operation of the device is intended to be functional. All values are referenced to GND and to a free ambient operating temperature of TA=25 ± 5°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{IN}, R_{ON} to AGND	Input Voltage, On time resistor to AGND	-0.3 to 43.5	V
EN, FB, SS to AGND	Enable, Feedback, soft-Start Input to AGND	-0.3 to 7.0	V
$V_{ESD-HBM}$	ESD, human body model (2)	-2000 to 2000	V
T_J	Junction temperature	150	°C
T_{ST}	Storage temperature	-65 to 150	°C

F RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN (3)	TYP (4)	MAX (3)	UNIT
V_{IN}	Input voltage	6	-	42	V
EN	Enable input	0	-	6.5	V
T_A	Ambient temperature range	-40	-	85	°C
T_J	Junction temperature range	-40	-	125	°C

G THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Thermal resistance junction to ambient(5)	19.3	°C/W
θ_{JC}	Thermal resistance junction to case, no air flow	1.9	°C/W
T_{SD}	Thermal shut down, junction temperature, rising	165	°C
$T_{SD-HYST}$	Thermal shut down hysteresis, falling	15	°C
T_{SOLR}	Soldering temperature reflow, leads(6)	245	°C

H ELECTRICAL SPECIFICATIONS

Limits are valid for recommended junction temperature range of -40°C to 125°C. Typical values represent the most likely norm at following conditions: V_{IN}=24V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
Specifications regarding supply voltage V_{IN}						
V_{IN}	Input voltage		6	24	42	V
Specifications regarding output voltage V_{OUT}						
V_{OUT}	Regulated output voltage	I_{OUT}=1.0A	0.8	-	6	V
I_{OCP}	Over current protection		2.3	2.6	3.65	A
Specifications regarding to pin EN Enable						
V_{EN}	Low level input voltage	V_{EN} falling	1.10	1.18	1.25	V
V_{EN-HYS}	EN input hysteresis		-	90	-	mV
Specifications regarding to the system						
f_{SW}	Switching frequency		0.2	-	0.8	MHz
t_{ON-MIN}	ON timer minimum pulse width		-	150	-	ns
t_{OFF}	OFF timer pulse width		-	260	-	ns
Specifications regarding to the soft-start						
I_{SS}	SS source current	V_{SS} = 0V	5	8	11	µA

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Limits are valid for recommended junction temperature range of -40°C to 125°C. Typical values represent the most likely norm at following conditions: V_{IN}=24V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
I_{SS-DIS}	SS discharge current		-	-200	-	µA
Specifications regarding to the regulation and over-voltage comparator						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V T_J = -40°C to 125°C I_{OUT} = 2A	0.784	0.804	0.825	V
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V T_J = 25°C I_{OUT} = 10mA	0.786	0.802	0.818	V
V_{FB-OVP}	Feedback over-voltage protection threshold		-	0.92	-	V
I_{FB}	Feedback input bias current		-	5	-	nA
I_Q	Non Switching Input Current	V_{FB}= 0.86V	-	1	-	mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0V	-	25	-	µA
Specifications regarding to the performance parameters						
ΔV_{OUT}	Output Voltage Ripple	V_{OUT}=5V, C_{OUT}=100µF 6.3V X7R	-	8	-	mV $_{PP}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16V to 42V, I_{OUT}=1A	-	0.01	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24V, I_{OUT} = 0A to 1A	-	1.5	-	mV/A
η	Efficiency	V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1A	-	86	-	%
η	Efficiency	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A	-	85	-	%

NOTES

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

(3) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(4) Typical numbers are at 25°C and represent the most likely parametric norm.

(5) 4 layer JEDEC Printed Circuit Board, 100 vias, 35µm Copper, No air flow.

(6) JEDEC J-STD020

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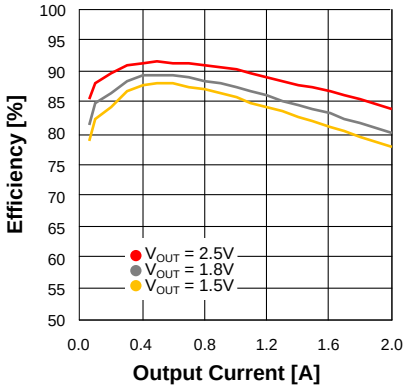
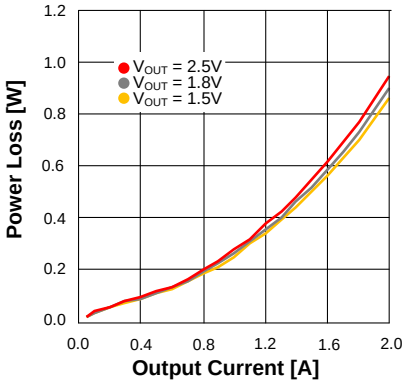
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R Ceramic; C_O = 100µF X7R Ceramic, T_{AMB} = 25°C

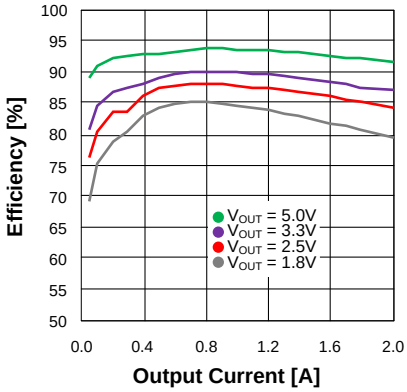
Efficiency: V_{IN} = 6V @ T_{AMB} = 25°C



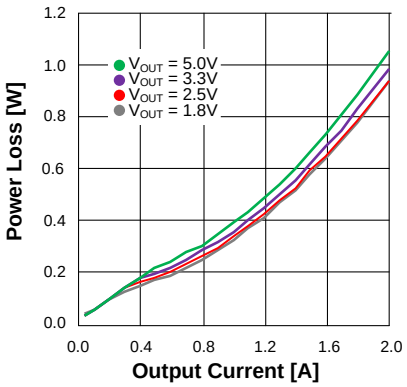
Power Loss: V_{IN} = 6V @ T_{AMB} = 25°C



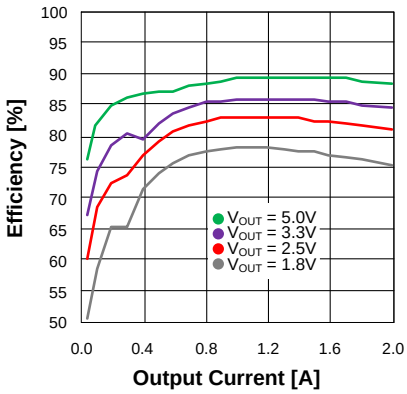
Efficiency: V_{IN} = 12V @ T_{AMB} = 25°C



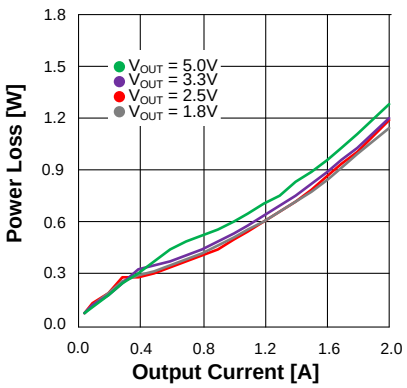
Power Loss: V_{IN} = 12V @ T_{AMB} = 25°C



Efficiency: V_{IN} = 24V @ T_{AMB} = 25°C



Power Loss: V_{IN} = 24V @ T_{AMB} = 25°C



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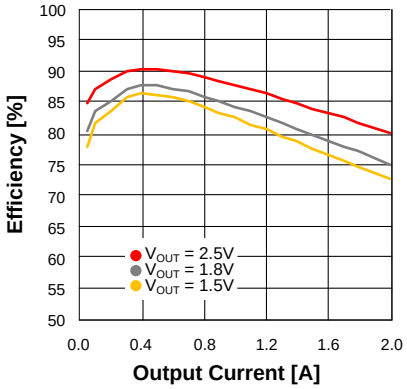
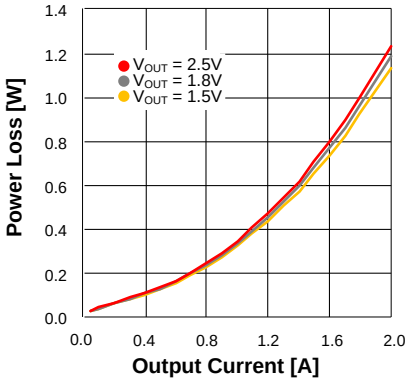
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R Ceramic; C_O = 100µF X7R Ceramic, T_{AMB} = 25°C

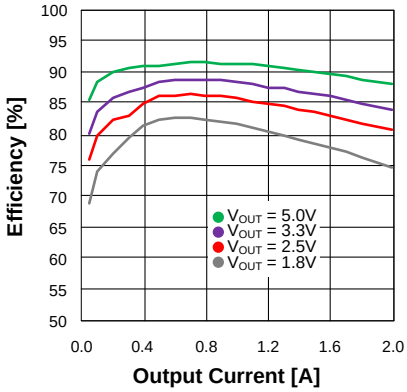
Efficiency: V_{IN} = 6V @ T_{AMB} = 85°C



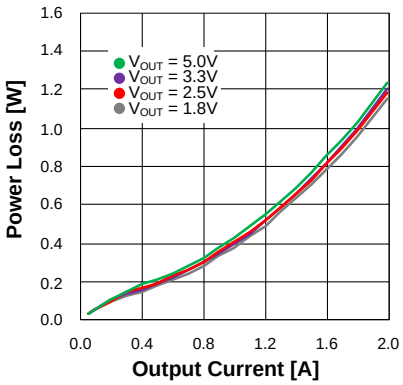
Power Loss: V_{IN} = 6V @ T_{AMB} = 85°C



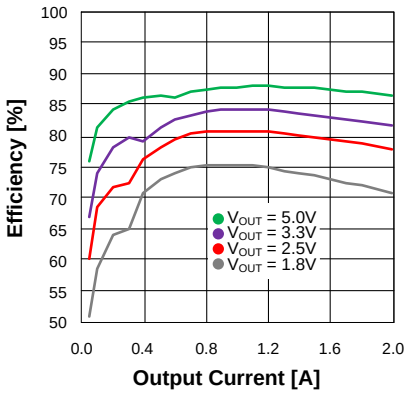
Efficiency: V_{IN} = 12V @ T_{AMB} = 85°C



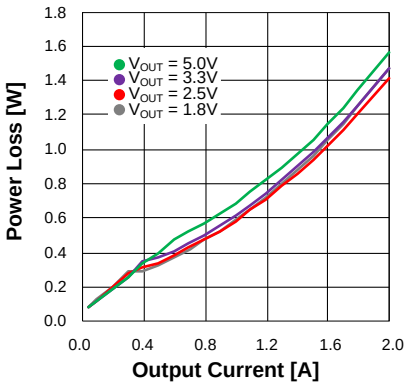
Power Loss: V_{IN} = 12V @ T_{AMB} = 85°C



Efficiency: V_{IN} = 24V @ T_{AMB} = 85°C



Power Loss: V_{IN} = 24V @ T_{AMB} = 85°C



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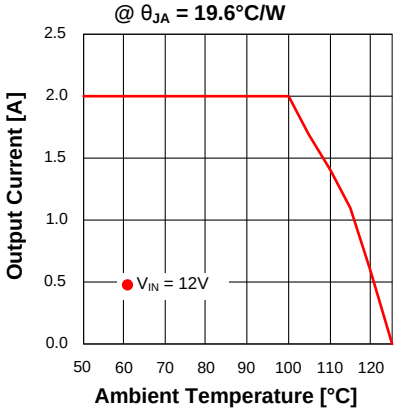
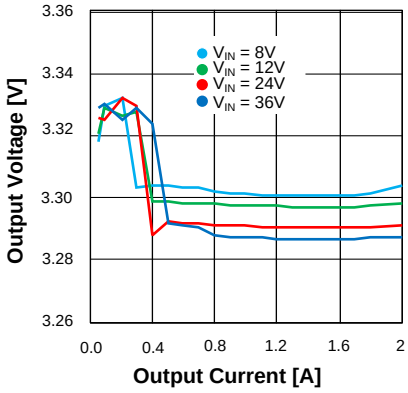
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R Ceramic; C_O = 100µF X7R Ceramic, T_{AMB} = 25°C

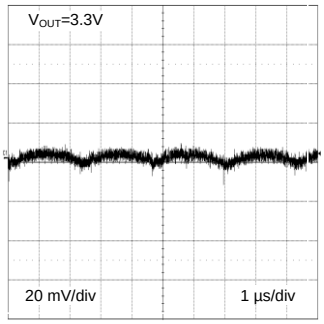
Thermal Derating: V_{OUT} = 3.3V @ θ_{JA} = 19.6°C/W



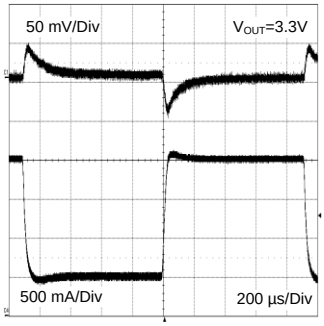
Line and Load Regulation T_{AMB} = 25°C



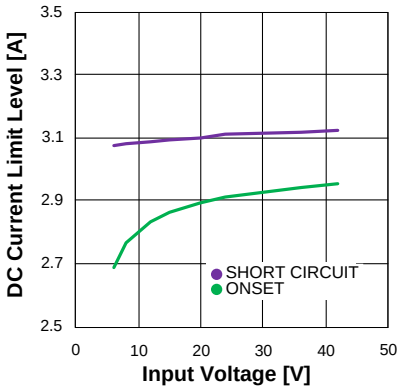
Output Rippel
V_{IN} = 24V, I_{OUT} = 2A, BW = 200MHz



Transient Response
V_{IN} = 24V, V_{OUT} = 3.3V, 0.6A to 2A Step



Current Limit vs. Input Voltage
V_{OUT} = 3.3V @ T_{AMB} = 25°C



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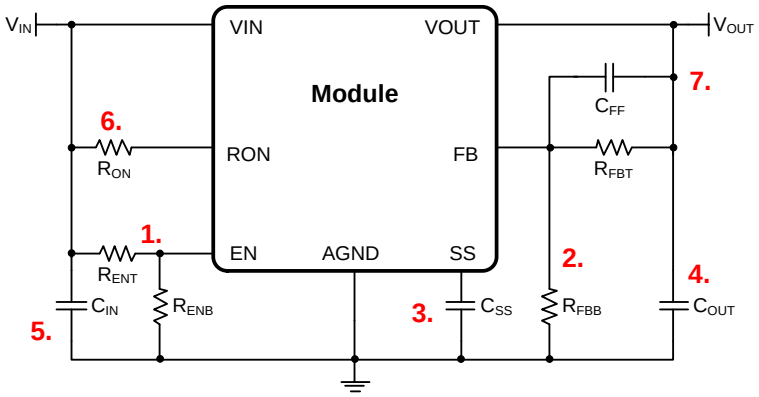
J CIRCUIT DESCRIPTION

MagI³C 7 Steps to design the power application

The next 7 simple steps will show how to select the external components to design your power application:

1. **Program under voltage lockout divider**
2. **Program output voltage**
3. **Select soft-start capacitor**
4. **Select output capacitor**
5. **Select input capacitor**
6. **Set operating frequency with R_{ON}**
7. **Select feed forward capacitor**



Step 1. Select Enable Divider, R_{ENT}, R_{ENB}

The enable input provides a precise 1.18V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typ) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the application block diagram is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. The two resistors should be chosen based on the following ratio:

$$\frac{R_{ENT}}{R_{ENB}} = \left(\frac{V_{IN\,-ENABLE}}{1.18V}\right) - 1 \qquad (1)$$

The EN pin is internally pulled up to V_{IN} and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will guarantee smooth startup and will prevent overloading the input supply.

Step 2. Select Output Voltage (V_{OUT})

Output voltage is determined by a divider of two resistors connected between V_{OUT} and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The high-side MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on time cycles will not occur.

The ratio of the feedback resistors for a desired output voltage is:

J CIRCUIT DESCRIPTION

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_{OUT}}{0.8V}\right) - 1 \qquad (2)$$

These resistors should be chosen from values in the range of 1kΩ to 50kΩ.
A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.
A table of values for R_{FBT}, R_{FBB}, and R_{ON} is included in the applications circuit.

Step 3. Select Soft-Start Capacitor (C_{SS})
Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot. Upon turn-on, after all UVLO conditions have been passed, an internal 8µA current source begins charging the external soft-start capacitor. The soft-start capacitor can be calculated with: This equation can be rearranged as follows:

$$C_{SS} = t_{SS} * \frac{8\mu A}{0.8V} \qquad (3)$$

with t_{ss} = select soft-start time in (ms)

Use of a 0.022µF capacitor results in 2.2ms soft-start duration. This is a recommended value. Note that high values of CSS capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use equation (15) below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018µF. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200µA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Over-current fault
- Internal V_{IN} UVLO

Step 4. Select Output Capacitor (C_{OUT})
None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case RMS current rating of $0.5 * I_{LR\,P-P}$, as calculated in equation (16) below. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

Capacitance:
The following equation provides a good first pass approximation of C_{OUT} for load transient requirements:

$$C_{OUT} \geq \frac{I_{STEP} * V_{FB} * L * V_{IN}}{(4 * V_{OUT} * (V_{IN} - V_{OUT}) * V_{OUT-TRAN})} \qquad (4)$$

For example:
$I_{STEP} = 2A, V_{IN} = 24V, V_{OUT} = 3.3V, V_{OUT-TRAN} = 50mV$
Solving:

$$C_{OUT} \geq \frac{2A * 0.8V * 10\mu H * 24V}{(4 * 3.3V * (24V - 3.3V) * 50mV)}$$

$$C_{OUT} \geq 28.1\mu F$$

ESR:
The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the over-voltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid over-voltage protection during normal operation. The following equations can be used:

J CIRCUIT DESCRIPTION

$$ESR_{MAX-RIPPLE} \leq \frac{V_{OUT-RIPPLE}}{I_{LR\ P-P}} \quad (5)$$

where $I_{LR\ P-P}$ is calculated using equation (16) below.

$$ESR_{MAX-OVP} < \frac{(V_{FB-OVP} - V_{FB})}{(I_{LR\ P-P} * A_{FB})} \quad (6)$$

where A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency.
As worst case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.
The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = \frac{I_{LR\ P-P}}{\sqrt{12}} \quad (7)$$

Step 5. Select Input Capacitor (C_{IN})
The MagI³C power module contains an internal 0.47µF input ceramic capacitor. Additional input capacitance is required external to the MagI³C power module to handle the input ripple current of the application. This input capacitance should be located as close as possible to the MagI³C power module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by the equation:

$$I(C_{OUT(RMS)}) \approxeq \frac{1}{2} * I_{OUT} * \sqrt{(D\ /\ 1-D)} \quad (8)$$

$$\text{where } D \approxeq \frac{V_{OUT}}{V_{IN}}$$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_{OUT}$).

Recommended minimum input capacitance is 10µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} * D * (1-D)}{f_{SW-CCM} * \Delta V_{IN}} \quad (9)$$

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 3.3V output application this equals 240 mV and f_{SW} = 400 kHz.

$$C_{IN} \geq \frac{2A * \frac{3.3V}{24V} * (1-\frac{3.3V}{24V})}{400000 * 0.240V}$$

$$C_{IN} \geq 2.5\mu F$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

Step 6. Select On-Time Resistor (R_{ON})
Many designs will begin with a desired switching frequency in mind. For that purpose the following equation can be used.

$$R_{ON} \approxeq \frac{V_{OUT}}{(1.3 * 10^{-10} * f_{SW(CCM)})} \quad (10)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the on-time and off-time for the COT control

J CIRCUIT DESCRIPTION

section. The on-time of the MagI³C power module timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = \frac{(1.3 * 10^{-10} * R_{ON})}{V_{IN}} \quad (11)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150ns. The on-timer has a limiter to ensure a minimum of 150ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{(V_{IN(MAX)} * 150ns)} \quad (12)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum on-time of 150ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} * 150nsec}{(1.3 * 10^{-10})} \quad (13)$$

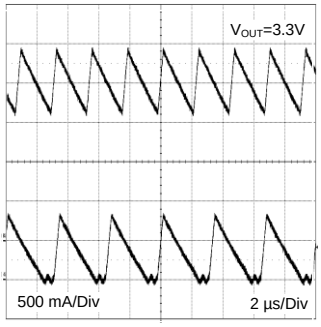
If R_{ON} calculated in equation (10) is less than the minimum value determined in equation (13) a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.
Additionally note, the minimum off-time of 260 ns limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

Discontinuous Conduction and Continuous Conduction Modes
At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency. Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \approx \frac{V_{OUT} * (V_{IN} - 1) * 10\mu H * 1.18 * 10^{20} * I_{OUT}}{(V_{IN} - V_{OUT}) * R_{ON^2}} \quad (14)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using equation (12) above.
Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

CCM and DCM Operating Modes
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A/0.32A



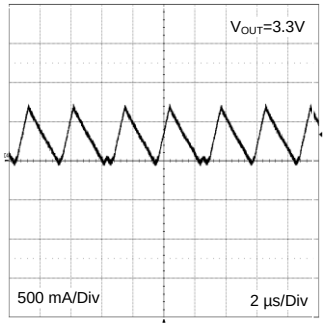
The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCM} \approx \frac{V_{OUT} * (V_{IN} - V_{OUT})}{(2 * 10\mu H * f_{SW(CCM)} * V_{IN})} \quad (15)$$

J CIRCUIT DESCRIPTION

Following is a typical waveform showing the boundary condition.

Transition Mode Operation
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0.35A



The inductor internal to the module is 10µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\,P-P} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{(10\mu H * f_{SW} * V_{IN})} \qquad (16)$$

Where V_{IN} is the maximum input voltage and f_{SW} is determined from equation (10).
If the output current I_{OUT} is determined by assuming that $I_{OUT} = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

Step 7. Select Feed Forward Capacitor (Cff)
As worst case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1. The selected capacitor should have sufficient voltage and RMS current rating.
The feed forward capacitor C_{FF}, should be located close to the FB pin.

Select Power Loss and Board thermal Requirements

For example:
$V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A, T_{AMB(MAX)} = 85°C$ and $T_J = 125°C$,
the device must see a maximum junction-to-ambient thermal resistance of:

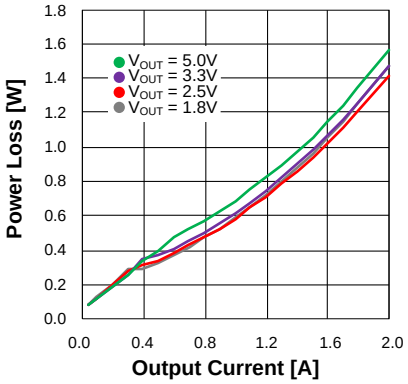
$$\theta_{CA} < \frac{(T_{J-MAX} - T_{AMB(MAX)})}{P_{IC-Loss}} - \theta_{JC} \qquad (17)$$

Given the typical thermal resistance from junction to case to be 1.9 °C/W. Use the 85°C power dissipation curves in the Typical Performance Characteristics section to estimate the PIC-LOSS for the application being designed. In this application it is 1.5W.

$$\theta_{CA} = \frac{(125°C - 85°C)}{1.5W} - 1.9°C/W = 24.8°C/W$$

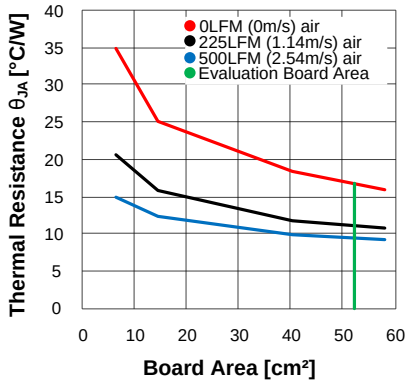
J CIRCUIT DESCRIPTION

Power Loss: V_{IN} = 24V @ T_{AMB} = 85°C



To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following package thermal resistance graph. This graph is taken from the typical performance characteristics section and shows how the θ_{JA} varies with the PCB area.

Package Thermal Resistance θ_{JA} 4 Layer Printed Circuit Board with 35µm Copper



For $\theta_{CA} < 24.8°C/W$ and only natural convection (i.e. no air flow), the PCB area can be smaller than 12cm^2. This corresponds to a square board with 3cm x 3cm copper area, 4 layers, and 35µm copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

PCB Layout Instructions:

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following five simple design rules.

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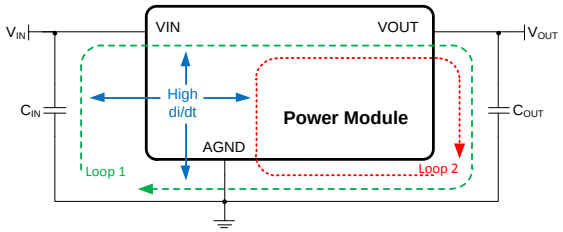
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

J CIRCUIT DESCRIPTION



1: Minimize area of switched current loops.
From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{in1}) is placed at a distance away from the MagI³C power module. Therefore place C_{IN1} as close as possible to the MagI³C power module V_{IN} and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad.

2: Have a single point ground.
The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to PGND.

3: Minimize trace length to the FB pin.
The feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the MagI³C power module to minimize noise pickup.

4: Make input and output bus connections as wide as possible.
This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5: Provide adequate device heat-sinking.
Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 254µm thermal vias spaced 1.5mm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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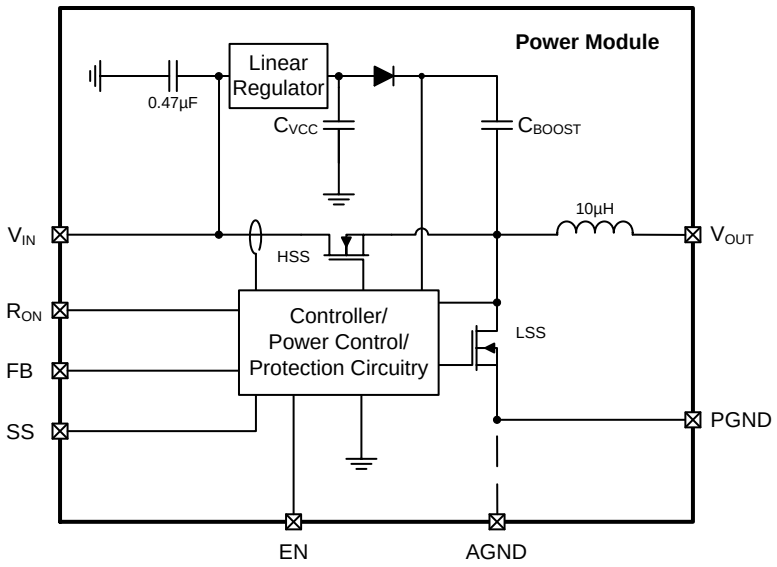
K BLOCK DIAGRAM



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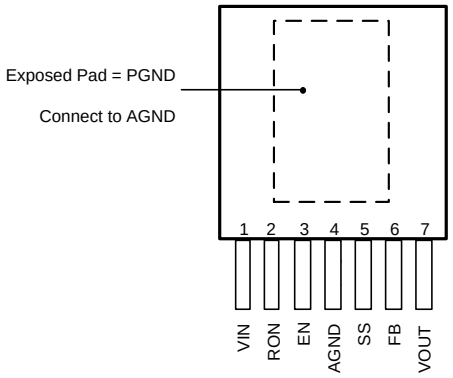
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

L PIN CONFIGURATION



Top View 7 pin PFM

M DETAILED PIN DESCRIPTION

PIN #	PIN SYMBOL	TYPE	PIN DESCRIPTION
1	V_{IN}	PWR	The supply input pin is a terminal for unregulated input voltage source. It is required to use a filtering capacitance nearby input voltage pin and PGND.
2	R_{ON}	I	An external resistor from V_{IN} to R_{ON} pin sets the on-time and frequency of the application. The value range of the resistor is from 25kΩ to 124kΩ.
3	EN	I	The enable input pin is connected to the precision enable comparator and the rising threshold is at 1.18V. Maximum recommended input level is 6.5V.
4	AGND	PWR	The analog ground pin is for all stated voltages the reference point and must be connected externally to PGND.
5	SS	I	For the soft-start function there is an internal 8µA current source which charges an external capacitor to generate the soft-start.
6	FB	I	The feedback pin is internally connected to the regulation amplifier, the over-voltage and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and AGND to set up the output voltage.
7	V_{OUT}	O	The output voltage pin is connected to the internal inductor. For the best stability and operation connect the output capacitor between this pin and PGND.
EP	EP	Exposed Pad	Exposed Pad – Internally connected to pin 4. Used to dissipate heat during operation. Must be electrically connected to pin 4 external to package

N PROTECTIVE FEATURES

OUTPUT OVER-VOLTAGE PROTECTION (OVP)

The voltage at FB is compared to a 0.92V internal reference. If FB rises above 0.92V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

OVER CURRENT PROTECTION (OCP)

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that DC current limit varies with duty cycle, switching frequency, and temperature.

OVER TEMPERATURE PROTECTION (OTP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165°C (typ.) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145°C (typ. Hyst = 20°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

ZERO COIL CURRENT DETECTION (ZCCT)

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

OUTPUT UNDER-VOLTAGE PROTECTION (UVP)

The MagI³C power module will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.

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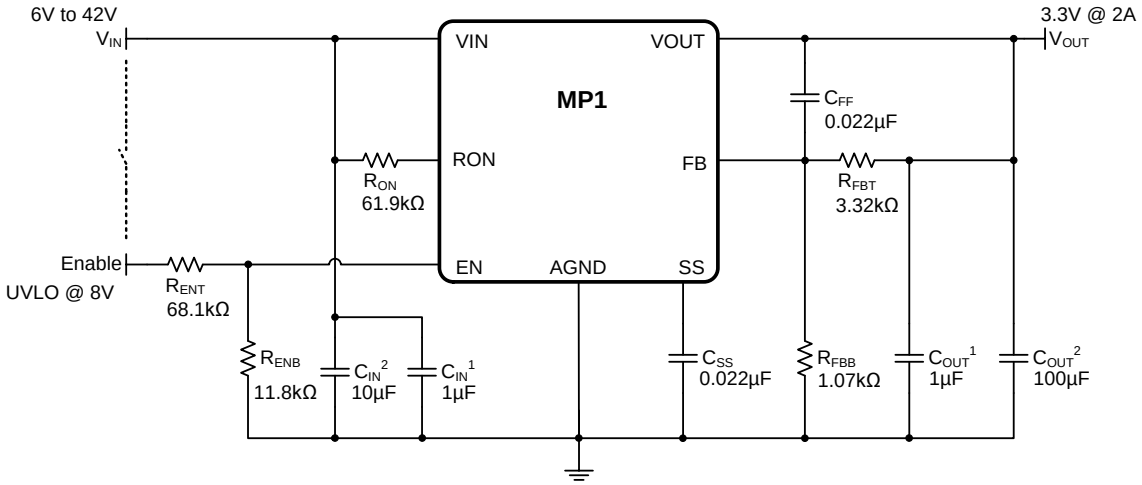
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

O APPLICATIONS

The MagI³C power module for high output voltage is easy-to-use DC-DC solutions capable of driving up to a 2A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. They are available in an innovative package that enhances thermal performance and allows for hand or machine soldering. Following application circuits show possible operating configurations.

O1 APPLICATIONS CIRCUIT



O1a Bill of Materials for Design Example 1:

Recommended component values: T_A = 25°C

Ref Design	Description	Case Size	Part
MP1	MagI³C Power Module	7 PIN PFM	WE MagI³C Power Module
C_{IN}^1, C_{OUT}^1	1µF, 50V, X7R, ±10%	1206	Capacitor
C_{IN}^2	10µF, 50V, X5R, ±20%	1210	Capacitor
C_{OUT}^2	100µF, 6,3V, X5R, ±20%	1210	Capacitor
C_{FF}	0.022µF, 100V, X7R, ±10%	0805	Capacitor
C_{SS}	0.022µF, 100V, X7R, ±10%	0805	Capacitor
R_{ENB}	11.8kΩ, ±1%	0805	Resistor
R_{ENT}	68.1kΩ, ±1%	0805	Resistor
R_{FBT}	3.32kΩ, ±1%	0805	Resistor
R_{FBB}	1.07kΩ, ±1%	0805	Resistor
R_{ON}	61.9kΩ, ±1%	0805	Resistor

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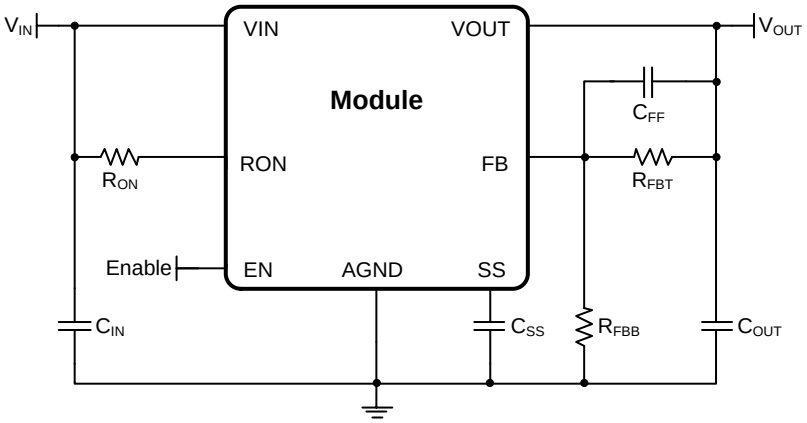
VDRM - Variable Step Down Regulator Module

O2 APPLICATIONS CIRCUIT



O2a Bill of Materials for Design Example 2:

Recommended component values: T_A = 25°C, I_{OUT} = 2A

V_{out}	5V	3.3V	2.5V	1.8V	1.5V	1.2V
R_{FBT}	5.62kΩ	3.32kΩ	2.26kΩ	1.87kΩ	1.00kΩ	4.22kΩ
R_{FBB}	1.07kΩ	1.07kΩ	1.07kΩ	1.5kΩ	1.13kΩ	8.45kΩ
R_{ON}	100kΩ	61.9kΩ	47.5kΩ	32.4kΩ	28.0kΩ	22.6kΩ
C_{IN}	10µF					
C_{OUT}	100µF					
C_{SS}	0.022µF					
C_{FF}	0.022µF					
V_{IN}	7.5-42V	6.5-42V	6-30V	6-25V	6-21V	6-19V

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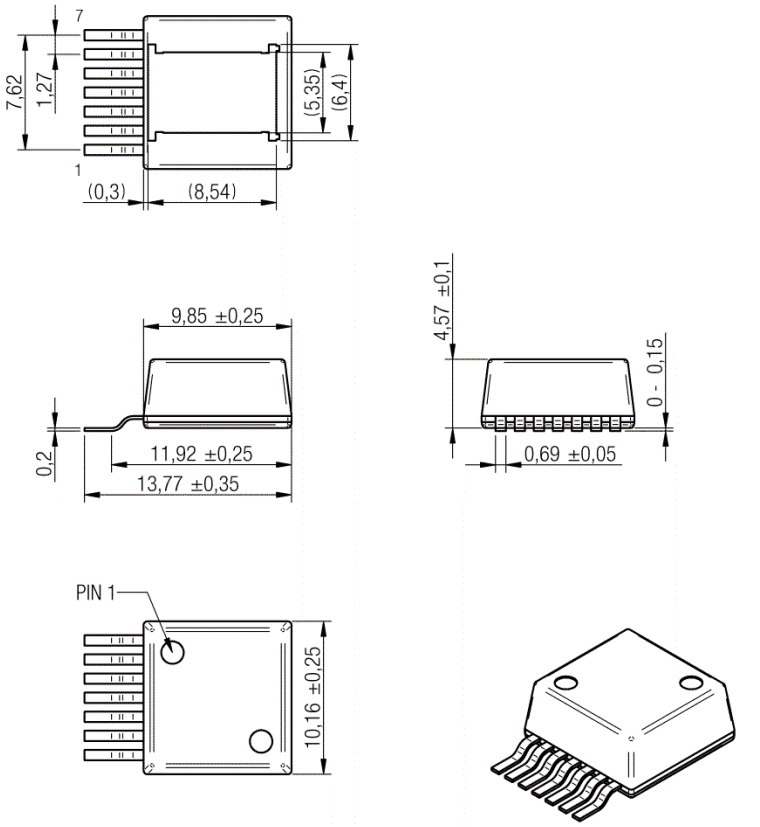
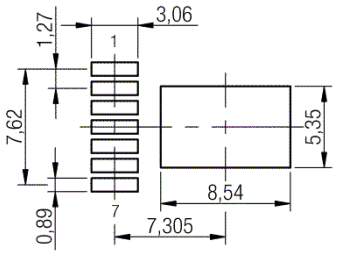
MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

P PHYSICAL DIMENSIONS (mm)



Scale - 2:1



Scale - 2:1

recommended soldering pad
solder past recommendation 150µm

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MagI³C Power Module Product Family
VDRM - Variable Step Down Regulator Module

Q DOCUMENT HYSTORY

DOCUMENT HISTORY

Revision	Date	Description
0.1	08.02.2013	Preliminary version
0.2	11.10.2013	Page 4: Efficiency fitted Page 7: Diagram Transient Response fitted Page 18: Schematic corrected

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MagI³C Power Module Product Family
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CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The disposal and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

If the product is potted in customer applications, the potting material might shrink during and after hardening. Accordingly to this the product is exposed to the pressure of the potting material with the effect that the body and termination is possibly damaged by this pressure and so the electrical as well as the mechanical characteristics are endanger to be affected. After the potting material is cured, the body and termination of the product have to be checked if any reduced electrical or mechanical functions or destructions have occurred.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Washing varnish agent that is used during the production to clean the application might damage or change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long turn function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to be complied with according to the technical reflow/ or wave soldering specification, otherwise no warranty will be sustained.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code, if not a 100% solderability can´t be warranted.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will result in the loss of warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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MagI³C Power Module Product Family
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IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that datasheet are current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
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