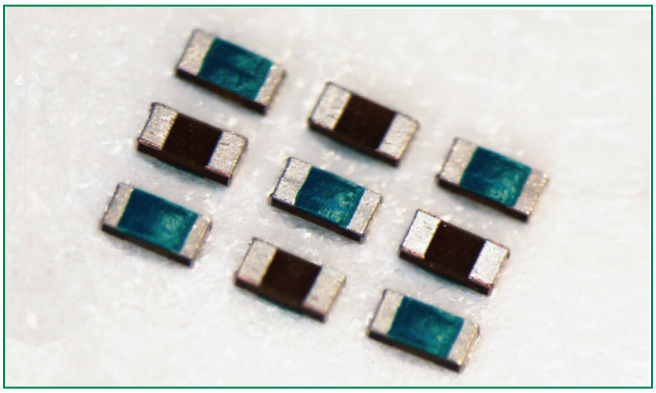
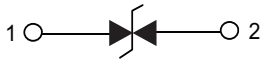
# RoHS Pb HF PGB2 Series Halogen Free / Lead-Free



## Equivalent Circuits




## Product Characteristics

| Part Number | Lines Protected | Component Package |
|---|---|---|
| PGB2010402KRHF | 1 | 0402 |

## Description

PulseGuard ESD Suppressors help protect sensitive electronic equipment against electrostatic discharge (ESD).

They use polymer composite materials to suppress fast-rising ESD transients (as specified in IEC 61000-4-2), while adding virtually no capacitance to the circuit.

They supplement the on-chip protection of integrated circuitry and are best suited for low-voltage, high-speed applications where low capacitance is important to ensure minimal interference of data signal integrity.

The new and ultra-small surface mount PGB2 0402 series offers a RoHS Compliant, Halogen Free, and 100% Lead Free circuit protection alternative.

## Features

- RoHS compliant
- Lead-free
- Halogen-free
- Ultra-low capacitance
- Low leakage current
- Fast response time
- One line of prtection
- Bi-directional
- Withstands multiple ESD strikes
- Compatible with pick-and-place processes

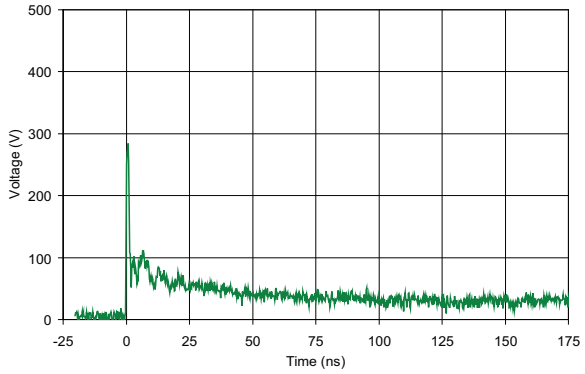
## Applications

- HDTV Hardware
- Laptop/Desktop Computer
- Network Hardware
- Computer Peripherals
- Digital Camera
- External Storage
- Set-Top Box
- Antenna

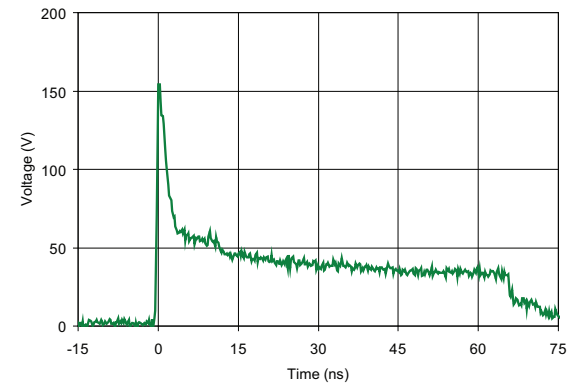
## Electrical Characteristics

| Specification | PGB2010402 | Notes |
|---|---|---|
| ESD Capability:<br>IEC 61000-4-2 Direct Discharge<br>IEC 61000-4-2 Air Discharge | <br>8kV<br>15kV | |
| Trigger Voltage (typical)<br>Clamping Voltage (typical) | 250V<br>40V | Measured per IEC 61000-4-2<br>8kV Direct Discharge Method |
| Trigger Voltage (typical)<br>Clamping Voltage (typical) | 150V<br>40V | Measured using 500 V TLP Direct Discharge Method |
| Rated Voltage (maximum) | 12VDC, max | |
| Capacitance (typical) | 0.07 pF, typical | Measured at 250 MHz |
| Response Time | <1nS | Measured per IEC 61000-4-2<br>8kV Direct Discharge Method |
| Leakage Current (typical) | <1nA | Measured at 12 VDC |
| ESD Pulse Withstand | 1000 pulses min | Some shifting in characteristics may occur when tested over multiple pulses at a very rapid rate |

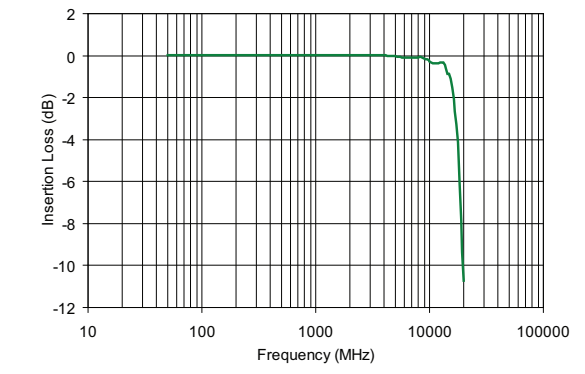
## Typical ESD Response Curve (8 kV IEC 61000-4-2 Direct Discharge)




## Typical TLP Response Curve (500 V Direct Discharge)

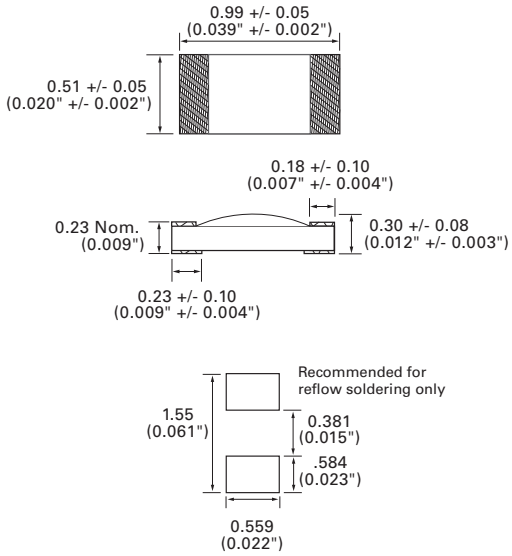



## Typical Insertion Loss




## Dimensions

Dimensions: mm (inch)



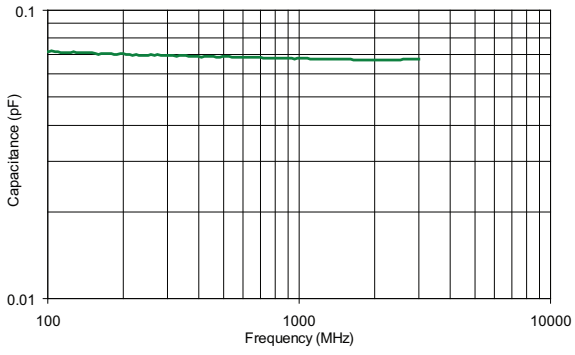

**Recommended Pad Layout**

## Part Numbering System

**PGB2 01 0402 KR HF**

- **PGB2** — **LEAD-FREE HALOGEN-FREE PULSEGUARD® ESD SUPPRESSORS**
- **01** — **LINES PROTECTED:** 01 = 1 line
- **0402** — **DEVICE SIZE CODE:** 0402 = 0402 (1005)
- **KR** — **QUANTITY & PACKAGING CODE:** KR = 10,000 pieces
- **HF** — **HALOGEN FREE**

## Typical Device Capacitance



## Physical Specifications

| | |
|---|---|
| **Materials** | Body: Epoxy / Glass Substrate<br>Terminations: Cu/Ni/Sn |
| **Device Weight** | 0.349 mg |
| **Solderability** | MIL-STD-202, Method 208 |
| **Soldering Parameters** | Wave solder - 260°C, 10 seconds maximum<br>Reflow solder - 260°C, 30 seconds maximum |

## Environmental Specifications

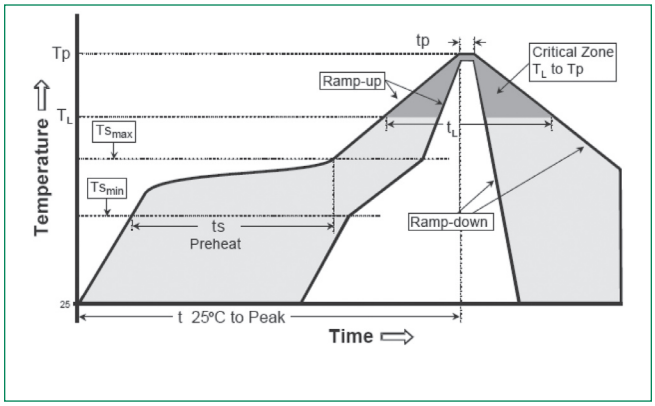
| | |
|---|---|
| **Operating Temperature** | -65°C to +125°C |
| **Biased Humity:**<br>**Biased Heat:** | 40°C, 95% RH, 1000 hours<br>85°C, 1000 hours |
| **Thermal Shock** | MIL-STD-202, Method 107G, -65°C to 125°C, 30 min. cycle, 10 cycles |
| **Vibration** | MIL-STD-202, Method 201A |
| **Chemical Resistance** | MIL-STD-202, Method 215 |
| **Solder Leach Resistance and Terminal Adhesion** | IPC/EIA J-STD-002 |

## Design Consideration

Because of the fast rise-time of the ESD transient, proper placement of PulseGuard suppressors are a key design consideration to achieving optimal ESD suppression. The devices should be placed on the circuit board as close to the source of the ESD transient as possible. Install PulseGuard suppressors (connected from signal/data line to ground) directly behind the connector so that they are the first board-level circuit component encountered by the ESD transient.

## Soldering Parameters

| | | |
|---|---|---|
| Reflow Condition | | Pb – Free assembly |
| Pre Heat | -Temperature Min ($T_{s(min)}$) | 150°C |
| | -Temperature Max ($T_{s(max)}$) | 200°C |
| | -Time (min to max) ($t_s$) | 60 – 180 seconds |
| Average ramp up rate (Liquidus Temp ($T_L$) to peak | | 3°C/second max |
| $T_{S(max)}$ to $T_L$ - Ramp-up Rate | | 3°C/second max |
| Reflow | -Temperature ($T_L$) (Liquidus) | 217°C |
| | -Temperature ($t_L$) | 60 – 150 seconds |
| Peak Temperature ($T_P$) | | 260°C |
| Time within 5°C of actual peak Temperature ($t_p$) | | 10 – 30 seconds |
| Ramp-down Rate | | 6°C/second max |
| Time 25°C to peak Temperature ($T_P$) | | 8 minutes max |



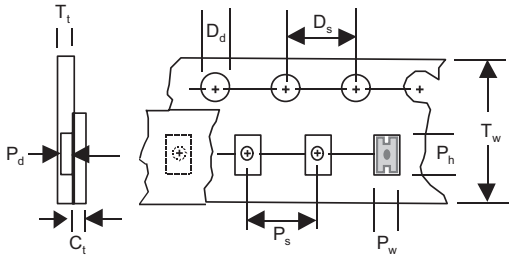

**Notes:**

- PGB2 Series recommended for reflow soldering only
- Recommended profile based on IPC/JEDED J-STD-020C
- For recommended soldering pad layout dimensions, please refer to Dimensions section of this data sheet

## Packaging

| Part Number | Quantity & Packaging Code | Quantity | Packaging Option | Packaging Specification |
|---|---|---|---|---|
| PGB2010402 | KR | 10000 | Tape & Reel (7" reel) | EIA RS-481-1 (IEC 286, part 3) |

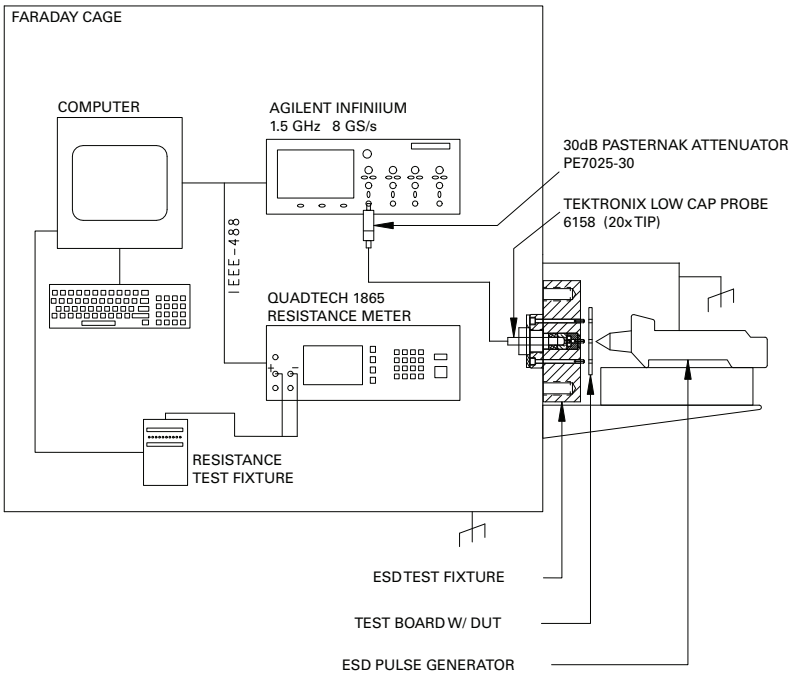
## Tape and Reel Specifications




**Carrier Tape:** 8mm, paper
**Reel:** 7" (178mm)

| Description | 0402 Series (mm) |
|---|---|
| $C_t$ - Cover tape thickness | 0.053 |
| $D_d$ - Drive hole diameter | 1.55 |
| $D_s$ - Drive hole spacing | 4.00 |
| $P_d$ - Pocket depth | 0.41 |
| $P_h$ - Pocket height | 1.12 |
| $P_s$ - Pocket spacing | 2.00 |
| $P_w$ - Pocket width | 0.62 |
| $T_t$ - Carrier tape thickness | 0.61 |
| $T_w$ - Carrier tape width | 8.00 |

## Typical ESD Pulse Test Setup




**Notes:**

- QuadQuadTech 1865 High Resistance Meter: Measures insulation resistance values
- KeyTek MiniZap ESD simulator with IEC tip: Simulates 8kV, direct discharge ESD event per IEC 61000-4-2
- Faraday cage: Shields the acquisition equipment from the electromagnetic fields generated by the simulator
- Agilent 2.25 GHz 54846A Oscilloscope: Records the voltage waveform from the device under test
- Tektronix 6158 probe with 30dB attenuator: Transmits the waveform from the device to the oscilloscope

## Characterization Methods for ESD Suppressors

Two of the most common methods used in industry for characterizing the performance of ESD suppressors are ESD transient testing, per IEC 61000-4-2 ESD waveform, and TLP. Since no standards exist for measurement and qualification of ESD suppressor performance, these two methods have become the de-facto standard for determining device trigger and clamp specifications. It is common to see trigger values to be based on the TLP method and clamping values based on the ESD transient method. Low voltage TLP obtained trigger values most closely resemble device DC turn-on .Since the two test methods are different and no method exists to accurately correlate suppressor response between the two test methods, trigger and clamp values should be specified for each method.

ESD transient testing, which is based on the IEC 61000-4-2 standard waveform, consists of subjecting a ESD suppressor to an subnanosecond risetime 8Kv transient generated by a commercial ESD simulator and recording trigger and clamp voltage levels. Clamp voltage level is obtained at 25ns. The basic ESD simulator circuit consists of a RC discharge network with R and C values of 330 ohms and 150 picofarads. Waveforms are captured using a 4 GHz oscilloscope(50 ohm input) with 20X resistive divider probes and a 30dB attenuator. Figures 1 and 2 show IEC current waveform and test setup.

Transmission line Pulse testing, commonly know as TLP testing consists of subjecting a ESD suppressor to a 50 ohm transmission line discharge pulse with a subnanosecond risetime and a pulse width of 65ns. Trigger values are obtained by varying the TLP voltage until a device trigger voltage is determined. Once the device is triggered, a clamp value is determined at 50ns. Waveforms are captured using a 4 GHz oscilloscope(50 ohm input) with 20X resistive divider probes and a 30dB attenuator. Figures 3 and 4 show a typical TLP voltage waveform and test setup.

It should be noted that no measurement standard exits for obtaining trigger and clamp voltage levels. Trigger and clamp values will vary from one test setup to another. Due to the subnanosecond risetime of ESD and TLP waveforms, any parasitic inductance and capacitance in the test system will affect measurements. Any effects due to inductance and capacitance need to be subtracted from the final measurement. It is important to remember that the test system will introduce a load across the ESD suppressor under test and this will also affect measurements. A high bandwidth 50 Ohm oscilloscope and probes(>1Ghz) need to be used for obtaining best results Attenuation values for the probe tip should be at least 20X in order to obtain high input impedance for measurements.

**Figure 1**

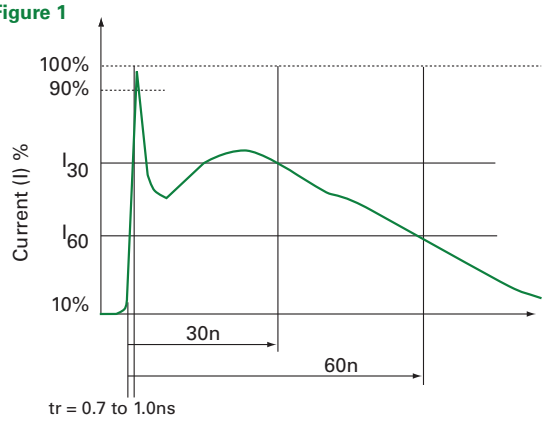



**Figure 2**

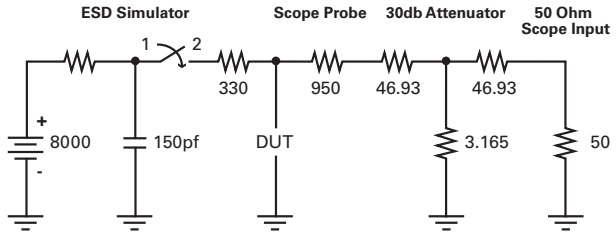



**Figure 3**

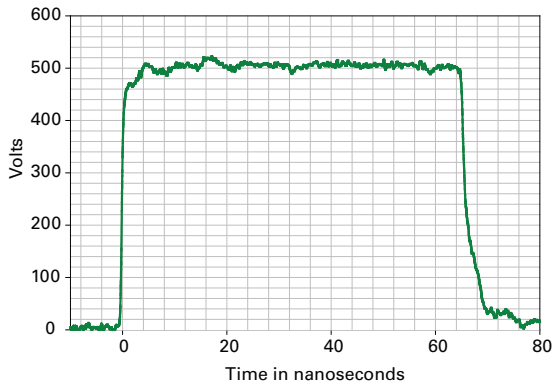



**Figure 4**