AT91SAM9263 Microcontroller Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding the Atmel® ARM® Thumb®-based AT91SAM9263 microcontroller.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM9263. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

6305C–ATARM–07-May-09

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM9263 Microcontroller on Atmel's Web site.

Table 2-1 gives the associated documentation needed to support full understanding of this application note.

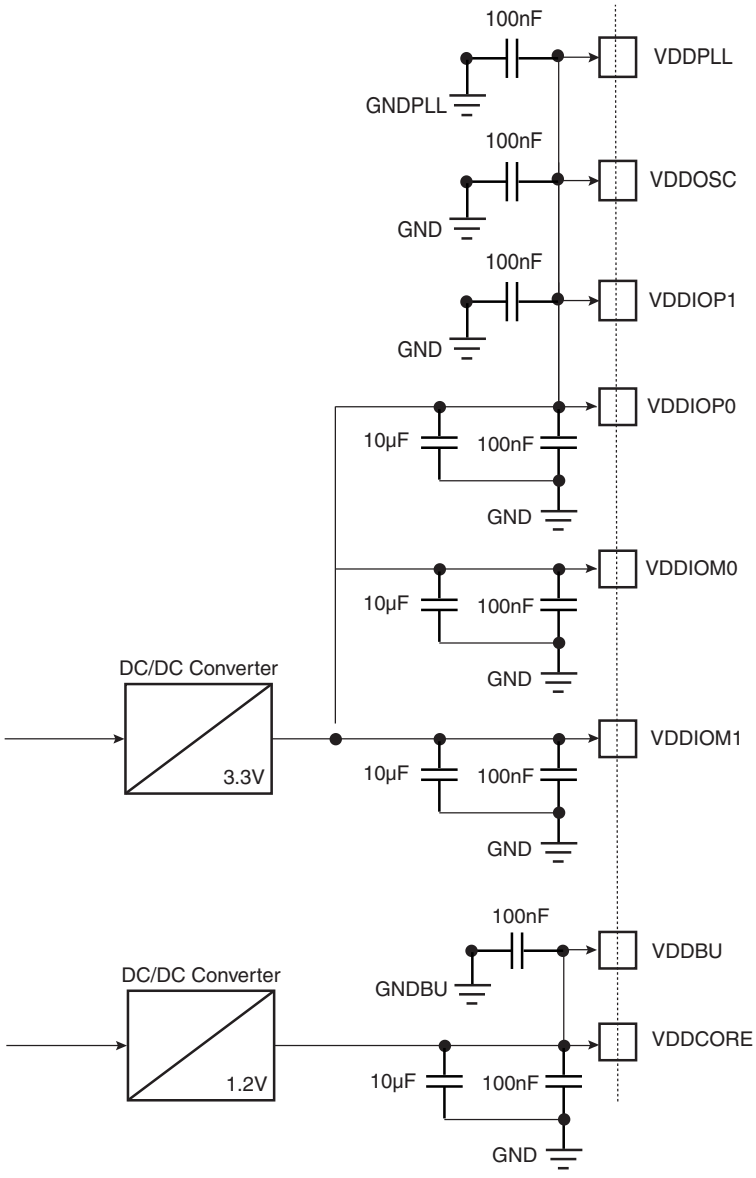
Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM9263 Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	AT91SAM9263-EK Evaluation Board User Guide
Using SDRAM on AT91SAM9 Microcontrollers	Using SDRAM on AT91SAM9 Microcontrollers
NANDFlash Support in AT91SAM9 Microcontrollers	NAND Flash Support in AT91SAM9 Microcontrollers

3. Schematic Check List

CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the Electrical Characteristics section in the datasheet to guarantee reliable operation of the device.

1.2V and 3.3V Dual Power Supply Schematic Example

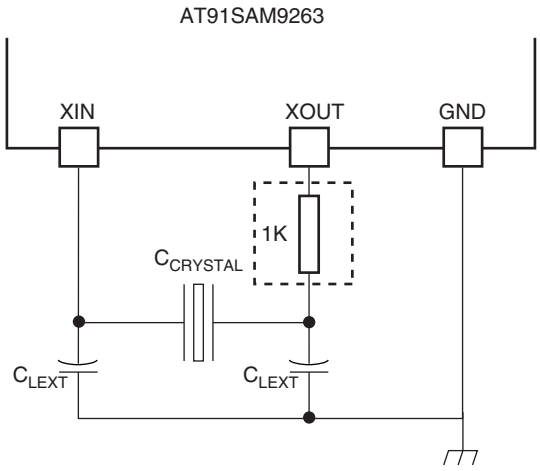
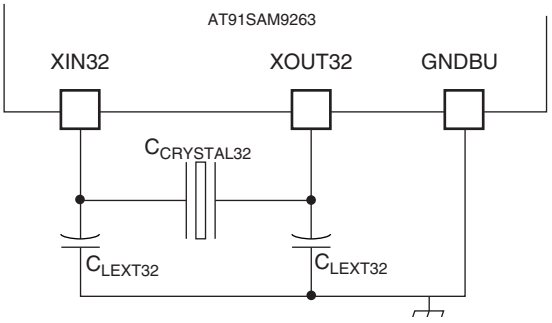


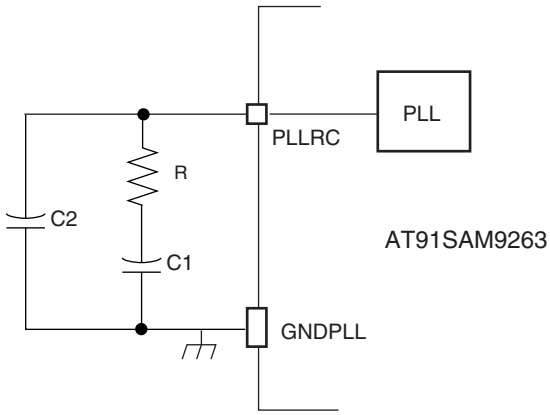
1.2V and 3.3V Dual Power Supply Schematic Example[1]

3.3V external memories (VDDIOM0 & VDDIOM1) - 3.3V Image Sensor (VDDIOP1) are used

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.08V to 1.32V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDBU	1.08V to 1.32V Decoupling capacitor (100 nF)[1][2]	Powers the Backup I/O lines (Slow Clock Oscillator and a part of the System Controller).
	VDDIOM0[3]	1.65V to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers first External Bus Interface (EBI0) I/O lines. Dual voltage range supported. The voltage ranges are selected by programming the VDDIOMSEL bit in the EBI0_CSA register. At power-up, the selected voltage is 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOM1[3]	1.65V to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers second External Bus Interface (EBI1) I/O lines. Dual voltage range supported. The voltage ranges are selected by programming the VDDIOMSEL bit in the EBI1_CSA register. At power-up, the selected voltage is 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP0[3][4]	2.7V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers Peripheral I/O lines and USB transceivers. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP1[3]	1.65V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers Peripheral I/O lines involving Image Sensor Interface (ISI). Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOSC	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the Main Oscillator.
	VDDPLL	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the PLL cells.

☑	Signal Name	Recommended Pin Connection	Description
	GND	Ground	GND pins are common to VDDCORE, VDDIOM, VDDOSC and VDDIOP pins. GND pins should be connected as shortly as possible to the system ground plane.
	GNDBU	Backup Ground	GNDBU pin is provided for VDDBU pin. GNDBU pin should be connected as shortly as possible to the system ground plane.
	GNDPLL	PLL Ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependent) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz. 470 Ohm resistor on XOUT is mandatory for crystals with frequencies above 8 MHz.	Crystal load capacitance to check ($C_{CRYSTAL}$).  Example: for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 15 pF, external capacitors are required: C_{LEXT} = 18pF. Refer to the electrical specifications of the AT91SAM9263 datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected	3.3V (VDDPLL) square wave signal External clock source up to 50 MHz Duty Cycle: 40 to 60% Refer to the electrical specifications of the AT91SAM9263 datasheet.
	XIN32 XOUT32 Slow Clock Oscillator	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Crystal load capacitance to check ($C_{CRYSTAL32}$).  Example: for an 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32}$= 12.5 pF, external capacitors are required: C_{LEXT32}= 17 pF. Refer to the electrical specifications of the AT91SAM9263 datasheet.

☑	Signal Name	Recommended Pin Connection	Description
	PLLRCA PLLRCB	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: “ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  AT91SAM9263 R, C1 and C2 must be placed as close as possible to the pins.

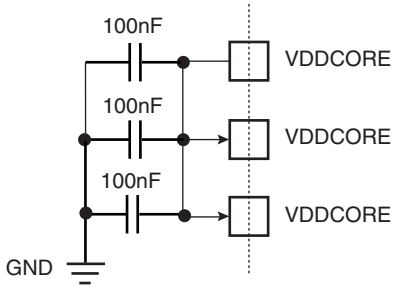
☑	Signal Name	Recommended Pin Connection	Description
ICE and JTAG[5]			
	TCK	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDO	Floating	Output driven at up to $V_{VDDIOP0}$
	RTCK	Floating	Output driven at up to $V_{VDDIOP0}$
	NTRST	Please refer to the I/O line considerations and the errata sections of AT91SAM9263 datasheet.	Internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm).
	JTAGSEL	**In harsh environments,[6] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDBU} to enter JTAG Boundary Scan. Internal pull-down resistor to GNDBU (15 kOhm).
Reset/Test			
	NRST	Application dependent. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm) is available for User Reset and External Reset control.
	TST	**In harsh environments,[6] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).**	Internal pull-down resistor to GNDBU (15 kOhm).
	BMS	Application dependent. Must be tied to $V_{VDDIOP0}$ to boot on Embedded ROM. Must be tied to GND to boot on external memory (EBI0 Chip Select 0). Must be stable during boot process.	Internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm). Need to isolate PB3/BMS during reset sequence if an external AC97 component is used: No access has to be done on AC97RX at reset.
Shutdown/Wakeup Logic			
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies. An external pull-up to VDDBU is needed and its value is to be higher than 1 MOhm. The resistor value is calculated according to the regulator enable implementation and the SHDN level.	The SHDN pin is a tri state output. No internal pull-up resistor. An external pull-up to VDDBU is needed. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).

☑	Signal Name	Recommended Pin Connection	Description
	WKUP	0V to $V_{VDDBU.}$	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).

☑	Signal Name	Recommended Pin Connection	Description
PIO			
	PAx PBx PCx PDx PEx	Application dependent.	All PIOs are pulled-up inputs at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals: PD12 (EBI0_A23), PD13 (EBI0_A24), PD14 (EBI0_A25). Rpullup (typ) = 100Kohm To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
EBI0 **9263 system boots only on EBI0 with dedicated Chip Select**			
	D0-D15 (D16-D31)	Application dependent.	Data Bus (D0 to D31) Data bus lines D0 to D15 are pulled-up inputs to $V_{VDDIOM0}$ at reset. Note: Data bus lines D16 to D31 are multiplexed with the PIOD controller. Their I/O line reset state is input with pull-up enabled too.
	A0-A22 (A23-A25)	Application dependent.	Address Bus (A0 to A25) All address lines are driven to '0' at reset. Note: EBI0_A23 (PD12), EBI0_A24 (PD13), EBI0_A25 (PD14) are enabled by default at reset through the PIO controllers.
EBI1			
	D0-D15 (D16-D31)	Application dependent.	Data Bus (D0 to D31) Data bus lines D0 to D15 are pulled-up inputs to $V_{VDDIOM1}$ at reset. Note: Data bus lines D16 to D31 are multiplexed with the PIOA controller. Their I/O line reset state is input with pull-up enabled too.
	A0-A22	Application dependent.	Address Bus (A0 to A22) All address lines are driven to '0' at reset.
SMC - SDRAM Controller - CompactFlash® Support - NANDFlash Support			
See "External Bus Interface (EBI) Hardware Interface" on page 13.			

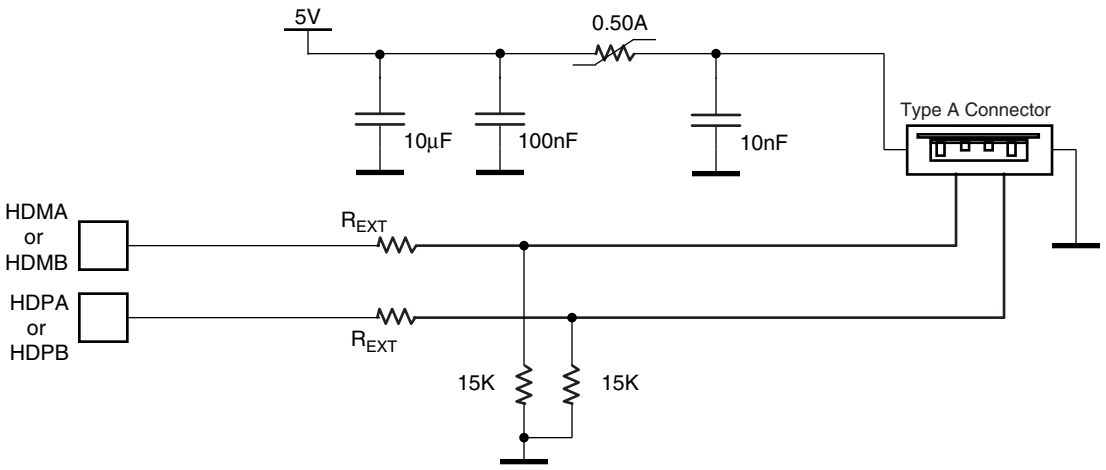
☑	Signal Name	Recommended Pin Connection	Description
USB Host (UHP)			
	HDPA HDPB	Application dependent.[7] Typically, 15 kOhm resistor to GND.	No internal pull-down resistors. To reduce power consumption, if USB Host is not used, connect HDPA/HDPB to GND.
	HDMA HDMB	Application dependent.[7] Typically, 15 kOhm resistor to GND.	No internal pull-down resistors. To reduce power consumption, if USB Host is not used, connect HDMA/HDMB to GND.
USB Device (UDP) **To reduce power consumption, USB Device Built-in Transceivers can be disabled (enabled by default).**			
	DDP	Application dependent.[8]	Integrated programmable pull-up resistor (UDP_TXVC) No internal pull-down resistor. To reduce power consumption, if USB Device is not used, connect DDP to $V_{VDDIOP0}$.
	DDM	Application dependent.[8]	No internal pull-down resistor. To reduce power consumption, if USB Device is not used, connect DDM to GND.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.

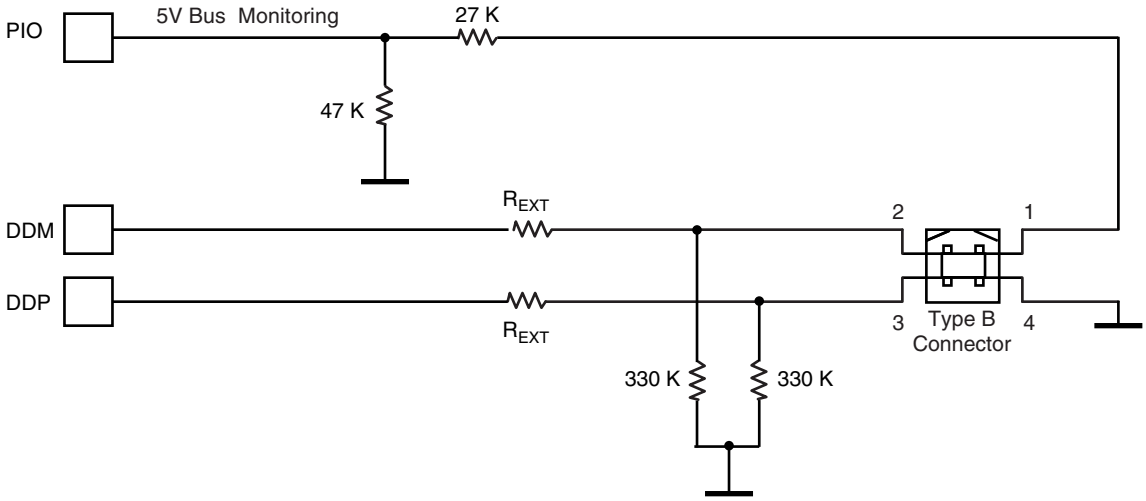


3. The double power supplies VDDIOM0, VDDIOM1, VDDIOP0 and VDDIOP1 power the device differently when interfacing with memories or with peripherals.
4. Some I/O lines of PIO Controller A and PIO Controller E are powered by VDDIOM1. See the sections “Multiplexing on PIO Controller A” and “Multiplexing on PIO Controller E” in the AT91SAM9263 datasheet**.** Some I/O lines of PIO Controller D are powered by VDDIOM0. See the section “Multiplexing on PIO Controller D” in the AT91SAM9263 datasheet**.**
5. It is recommended to establish accessibility to a JTAG connector for debug in any case.
6. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.

7. Example of USB Host connection:
   A termination serial resistor (R_{EXT}) must be connected to HDPA/HDPB and HDMA/HDMB. A recommended resistor value is defined in the electrical specifications of the AT91SAM9263 datasheet.



8. Example of USB Device connection:
   As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up.
   To prevent over consumption when the host is disconnected, an external pull-down can be added to DDP and DDM.
   A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM9263 datasheet.



4. External Bus Interface (EBI) Hardware Interface

Table 4-1 and Table 4-2 detail the connections to be applied between the EBI pins and the external devices for each Memory Controller:

Table 4-1. EBI Pins and External Static Devices Connections

Signals: EBI0_, EBI1_	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	**SMC**					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB(3)	BE0(6)
A1/NWR2/NBS2	A1	A0	A0	WE(2)	NLB(4)	BE2(6)
A2 - A22	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25(5)	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2(5)	CS	CS	CS	CS	CS	CS
NCS2/NANDCS(7)	CS	CS	CS	CS	CS	CS
NCS3/NANDCS(5)	CS	CS	CS	CS	CS	CS
NCS4/CFCS0(5)	CS	CS	CS	CS	CS	CS
NCS5/CFCS1(5)	CS	CS	CS	CS	CS	CS
NRD/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE(1)	WE	WE(2)	WE	WE
NWR1/NBS1	–	WE(1)	NUB	WE(2)	NUB(3)	BE1(6)
NWR3/NBS3	–	–	–	WE(2)	NUB(4)	BE3(6)

Notes:
1. NWR1 enables upper byte writes. NWR0 enables lower byte writes.
2. NWRx enables corresponding byte x writes. (x = 0,1,2 or 3)
3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
5. EBI0 signals only.
6. BEx: Byte x Enable (x = 0,1,2 or 3).
7. EBI1 signals only.

Table 4-2. EBI Pins and External Devices Connections

Signals: EBI0_, EBI1_	Pins of the Interfaced Device			
	SDRAM[8]	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NANDFlash[9]
Controller	**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0-I/O7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8-I/O15[5]
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21/NANDALE	–	–	–	ALE
A22/NANDCLE	–	REG	REG	CLE
A23 - A24[3]	–	–	–	–
A25[3]	–	CFRNW[1]	CFRNW[1]	–
NCS0	–	–	–	–
NCS1/SDCS	CS	–	–	–
NCS2[3]	–	–	–	–
NCS2/NANDCS[4]	–	–	–	–
NCS3/NANDCS[3]	–	–	–	CE[6]
NCS4/CFCS0[3]	–	CFCS0[1]	CFCS0[1]	–
NCS5/CFCS1[3]	–	CFCS1[1]	CFCS1[1]	–
NANDOE	–	–	–	OE
NANDWE	–	–	–	WE
NRD/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFCE1[3]	–	CE1	CS0	–
CFCE2[3]	–	CE2	CS1	–

Table 4-2. EBI Pins and External Devices Connections (Continued)

Signals: EBI0_, EBI1_	**Pins of the Interfaced Device**			
	SDRAM[8]	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NANDFlash[9]
Controller	**SDRAMC**	**SMC**		
SDCK	CLK	–	–	–
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT[7]	–	WAIT	WAIT	–
Pxx[2]	–	CD1 or CD2	CD1 or CD2	–
Pxx[2]	–	–	–	CE[6]
Pxx[2]	–	–	–	RDY

Notes:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
2. Any PIO line.
3. EBI0 signals only
4. EBI1 signals only
5. I/O8 - I/O15 bits used only for 16-bit NANDFlash.
6. CE connection depends on the NANDFlash.
   For standard NANDFlash devices, it must be connected to any free PIO line.
   For “CE don’t care” NANDFlash devices, it can be connected either to NCS3/NANDCS or to any free PIO line.
7. EBI0_NWAIT signal is multiplexed with PD5. EBI1_NWAIT signal is multiplexed with PE20.
8. For SDRAM connection examples, see Using SDRAM on AT91SAM9 Microcontrollers application note.
9. For NANDFlash connection examples, see NAND Flash Support in AT91SAM Microcontrollers application note.

5. AT91SAM Boot Program Hardware Constraints

See the AT91SAM Boot Program section of the AT91SAM9263 datasheet for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals (MHz)

3.0	3.2768	3.6864	3.84	4.0
4.433619	4.608	4.9152	5.0	5.24288
6.0	6.144	6.4	6.5536	7.159090
7.3728	7.864320	8.0	9.8304	10.0
11.05920	12.0	12.288	13.56	14.31818
14.7456	16.0	17.734470	18.432	20.0

5.2 SAM-BA™ Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-1. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PC30
DBGU	DTXD	PC31

5.3 DataFlash® Boot

The DataFlash Boot program searches for a valid application in the SPI DataFlash memory.

The DataFlash must be connected to NPCS0 of the SPI0.

Table 5-2. Pins Driven during DataFlash Boot Program Execution

Peripheral	Pin	PIO Line
SPI0	MOSI	PA1
SPI0	MISO	PA0
SPI0	SPCK	PA2
SPI0	NPCS0	PA5

5.4 SD Card Boot

The SD Card Boot program searches for a valid application in the SD Card memory.

Table 5-3. Pins Driven during SD Card Boot Program Execution

Peripheral	Pin	PIO Line
MCI1	MCCK	PA6
MCI1	MCCDA	PA7
MCI1	MCDA0	PA8
MCI1	MCDA1	PA9
MCI1	MCDA2	PA10
MCI1	MCDA3	PA11

SD Card Boot support depends on component version. Refer to the AT91SAM9263 datasheet.

5.5 NANDFlash Boot

The NANDFlash Boot program searches for a valid application in the NANDFlash memory.

Table 5-4. Pins Driven during NANDFlash Boot Program Execution

Peripheral	Pin	PIO Line
PIOD	PIO (for NAND Chip Select)	PD15
PIOA	PIO (for NAND Ready Busy)	PA22
Address Bus	NANDCLE	A22
Address Bus	NANDALE	A21

NANDFlash Boot support depends on component revision. Refer to the AT91SAM9263 datasheet.

6. Revision History

Doc. Rev	Comments	Change Request Ref.
6305C	Add a line to XIN and XOUT pins in "Schematic Check List" table Add a Caution paragraph before "Schematic Check List" table Edit SHDN line in "Schematic Check List" table	6327 6124 6149
6305B	EBI0/EBI1 specified for signals NCS2 and NCS2/NANDCS Table 4-1 on page 13 Updated Recommended Pin Connection for "JTAGSEL" and "TST"	4588 5076
6305A	First issue	

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