

250MHz Differential Twisted-Pair Drivers

The EL5171 and EL5371 are single and triple bandwidth amplifiers with an output in differential form. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The input signal is single-ended and the outputs are always differential.

On the EL5171 and EL5371, two feedback inputs provide the user with the ability to set the gain of each device (stable at minimum gain of one). For a fixed gain of two, please see EL5170 and EL5370.

The output common mode level for each channel is set by the associated V_{REF} pin, which have a -3dB bandwidth of over 50MHz. Generally, these pins are grounded but can be tied to any voltage reference.

All outputs are short circuit protected to withstand temporary overload condition.

The EL5171 and EL5371 are specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5171IS	5171IS	-	8 Ld SO	MDP0027
EL5171IS-T7	5171IS	7"	8 Ld SO	MDP0027
EL5171IS-T13	5171IS	13"	8 Ld SO	MDP0027
EL5171ISZ (See Note)	5171ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL5171ISZ-T7 (See Note)	5171ISZ	7"	8 Ld SO (Pb-free)	MDP0027
EL5171ISZ-T13 (See Note)	5171ISZ	13"	8 Ld SO (Pb-free)	MDP0027
EL5371IU	5371IU	-	28 Ld QSOP	MDP0040
EL5371IU-T7	5371IU	7"	28 Ld QSOP	MDP0040
EL5371IU-T13	5371IU	13"	28 Ld QSOP	MDP0040
EL5371IUZ (See Note)	5371IUZ	-	28 Ld QSOP (Pb-free)	MDP0040
EL5371IUZ-T7 (See Note)	5371IUZ	7"	28 Ld QSOP (Pb-free)	MDP0040
EL5371IUZ-T13 (See Note)	5371IUZ	13"	28 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

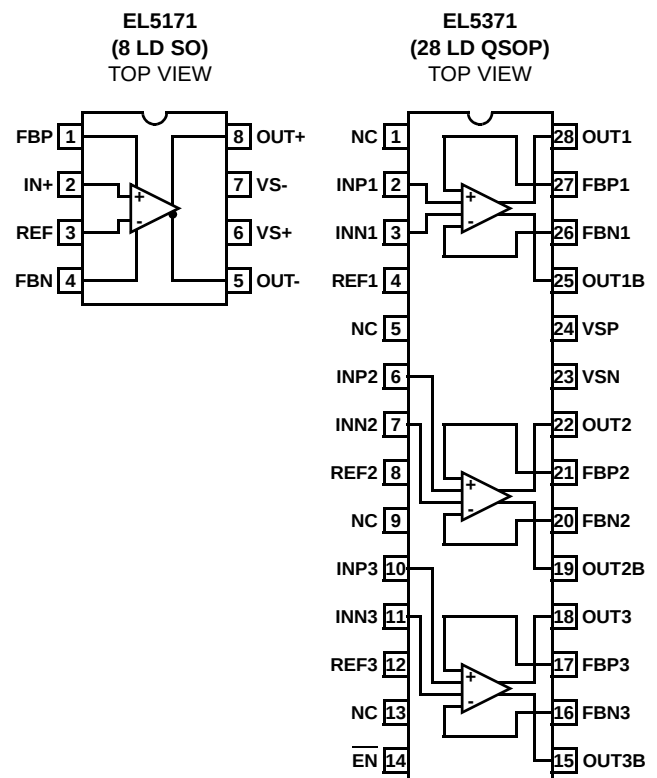
Features

- Fully differential outputs and feedback
- Input range $\pm 2.3V$ typ.
- 250MHz 3dB bandwidth
- 800V/ μs slew rate
- Low distortion at 5MHz
- Single 5V or dual $\pm 5V$ supplies
- 90mA maximum output current
- Low power - 8mA per channel
- Pb-free plus anneal available (RoHS compliant)

Applications

- Twisted-pair driver
- Differential line driver
- VGA over twisted-pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Pinouts



EL5171, EL5371

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_{S+} to V_{S-})12V
 Maximum Output Current ±60mA
 Storage Temperature Range-65°C to +150°C

Operating Junction Temperature +135°C
 Ambient Operating Temperature-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

Electrical Specifications V_{S+} = +5V, V_{S-} = -5V, T_A = 25°C, V_{IN} = 0V, R_{LD} = 1kΩ, R_F = 0, R_G = OPEN, C_{LD} = 2.7pF, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		250		MHz
		A _V = 2, R _F = 500, C _{LD} = 2.7pF		60		MHz
		A _V = 10, R _F = 500, C _{LD} = 2.7pF		10		MHz
BW	±0.1dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		50		MHz
SR	Slew Rate (EL5171)	V _{OUT} = 3V _{P-P} , 20% to 80%	600	800	1000	V/μs
	Slew Rate (EL5371)	V _{OUT} = 3V _{P-P} , 20% to 80%	540	700	1000	V/μs
T _{STL}	Settling Time to 0.1%	V _{OUT} = 2V _{P-P}		10		ns
T _{OVR}	Output Overdrive Recovery Time			20		ns
GBWP	Gain Bandwidth Product			100		MHz
V _{REFBW} (-3dB)	V _{REF} -3dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		50		MHz
V _{REFSR+}	V _{REF} Slew Rate - Rise	V _{OUT} = 2V _{P-P} , 20% to 80%		90		V/μs
V _{REFSR-}	V _{REF} Slew Rate - Fall	V _{OUT} = 2V _{P-P} , 20% to 80%		50		V/μs
V _N	Input Voltage Noise	at 10kHz		26		nV/√Hz
I _N	Input Current Noise	at 10kHz		2		pA/√Hz
HD2	Second Harmonic Distortion	V _{OUT} = 2V _{P-P} , 5MHz		-94		dBc
		V _{OUT} = 2V _{P-P} , 20MHz		-94		dBc
HD3	Third Harmonic Distortion	V _{OUT} = 2V _{P-P} , 5MHz		-77		dBc
		V _{OUT} = 2V _{P-P} , 20MHz		-75		dBc
dG	Differential Gain at 3.58MHz	R _L = 300Ω, A _V = 2		0.1		%
dθ	Differential Phase at 3.58MHz	R _L = 300Ω, A _V = 2		0.5		°
e _S	Channel Separation	at f = 1MHz		90		dB
INPUT CHARACTERISTICS						
V _{OS}	Input Referred Offset Voltage			±1.5	±25	mV
I _{IN}	Input Bias Current (V _{IN+} , V _{IN-})		-14	-6	-3	μA
I _{REF}	Input Bias Current (V _{REF})		0.5	1.3	4	μA
R _{IN}	Differential Input Resistance			300		kΩ
C _{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Mode Input Range		±2.1	±2.3	±2.5	V
CMIR+	Common Mode Positive Input Range at V _{IN+} , V _{IN-}	Tested only for EL5371	3.1	3.4		V
CMIR-	Common Mode Negative Input Range at V _{IN+} , V _{IN-}	Tested only for EL5371		-4.5	-4.2	V
V _{REFIN +}	Positive Reference Input Voltage Range (EL5371)	V _{IN+} = V _{IN-} = 0V	3.5	±3.8		V

EL5171, EL5371

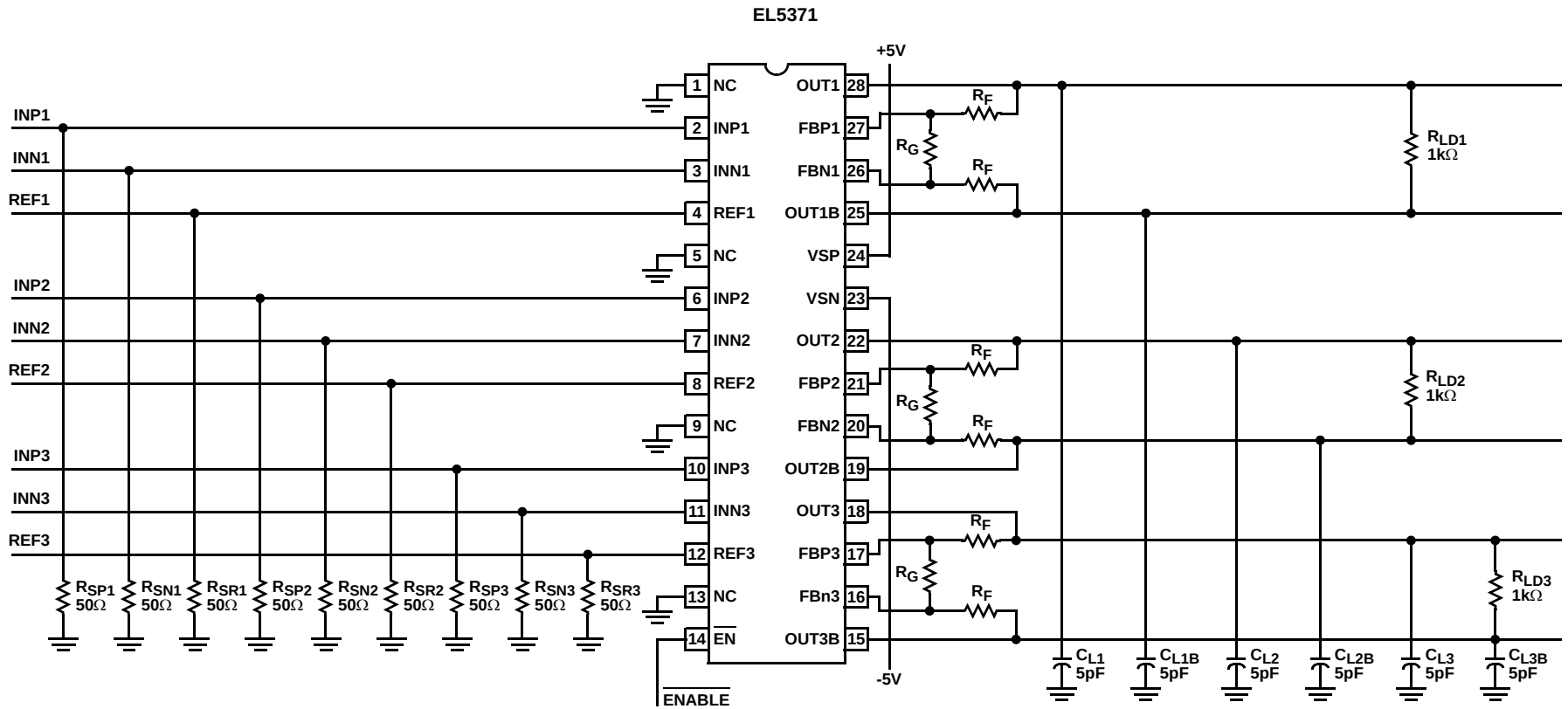
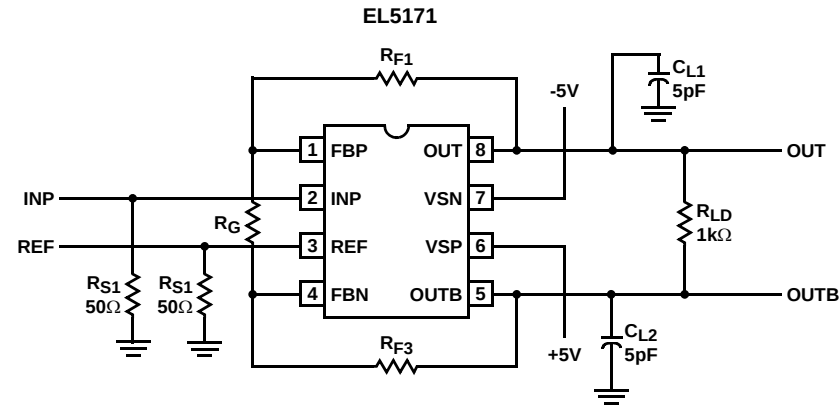
Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $T_A = 25^{\circ}C$, $V_{IN} = 0V$, $R_{LD} = 1k\Omega$, $R_F = 0$, $R_G = OPEN$, $C_{LD} = 2.7pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V _{REFIN} -	Negative Reference Input Voltage Range (EL5371)	V _{IN} + = V _{IN} - = 0V		-3.3	-3	V
V _{REFOS}	Output Offset Relative to V _{REF} (EL5371)			±60	±100	mV
CMRR	Input Common Mode Rejection Ratio (EL5371)	V _{IN} = ±2.5V	70	82		dB
Gain	Gain Accuracy	V _{IN} = 1 (EL5171)	0.981	0.996	1.011	V
		V _{IN} = 1 (EL5371)	0.978	0.993	1.008	V
OUTPUT CHARACTERISTICS						
V _{OUT}	Output Voltage Swing	R _L = 500Ω to GND (EL5171)		±3.4		V
		R _L = 500Ω to GND (EL5371)	±3.6	±3.9		V
I _{OUT} (Max)	Maximum Output Current	R _L = 10Ω, V _{IN} = ±3.24 (EL5171)	±70	±90	±120	mA
		R _L = 10Ω, V _{IN} = ±3.24 (EL5371)	±50	±70	±90	mA
R _{OUT}	Output Impedance			130		mΩ
SUPPLY						
V _{SUPPLY}	Supply Operating Range	V _S + to V _S -	4.75		11	V
I _S (ON)	Power Supply Current - Per Channel		6.8	7.5	8.2	mA
I _S (OFF)+	Positive Power Supply Current - Disabled (EL5371)	$\overline{EN}$ pin tied to 4.8V		1.7	10	μA
I _S (OFF)-	Negative Power Supply Current - Disabled (EL5371)		-200	-120		μA
PSRR	Power Supply Rejection Ratio	V _S from ±4.5V to ±5.5V (EL5171)	70	84		dB
		V _S from ±4.5V to ±5.5V (EL5371)	65	83		dB
ENABLE (EL5371 ONLY)						
t _{EN}	Enable Time			215		ns
t _{DS}	Disable Time			0.95		μs
V _{IH}	$\overline{EN}$ Pin Voltage for Power-Up				V _S + - 1.5	V
V _{IL}	$\overline{EN}$ Pin Voltage for Shut-Down		V _S + - 0.5			V
I _{IH-EN}	$\overline{EN}$ Pin Input Current High	At V _{EN} = 5V		122	130	μA
I _{IL-EN}	$\overline{EN}$ Pin Input Current Low	At V _{EN} = 0V	-10	-8		μA

Pin Descriptions

EL5171	EL5371	PIN NAME	PIN FUNCTION
1	17, 21, 27	FBP1, 2, 3	Feedback from non-inverting output
2	2, 6, 10	INP1, 2, 3	Non-inverting inputs
3	3, 7, 11	INN1, 2, 3	Inverting inputs, note that on EL5171, this pin is also the REF pin
4	16, 20, 26	FBN1, 2, 3	Feedback from inverting output
5	15, 19, 25	OUT1B, 2B, 3B	Inverting outputs
6	24	VSP	Positive supply
7	23	VSN	Negative supply
8	18, 22, 28	OUT1, 2, 3	Non-inverting outputs
	1, 5, 9, 13	NC	No connects, grounded for best crosstalk performance
	4, 8, 12	REF1, 2, 3	Reference input, sets common-mode output voltage
	14	$\overline{EN}$	ENABLE

Connection Diagrams



EL5171, EL5371

Typical Performance Curves

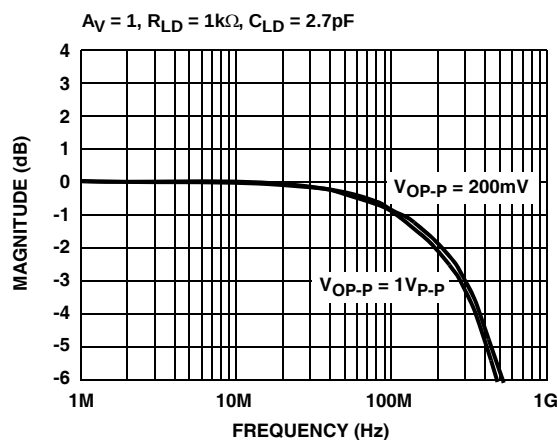


FIGURE 1. FREQUENCY RESPONSE

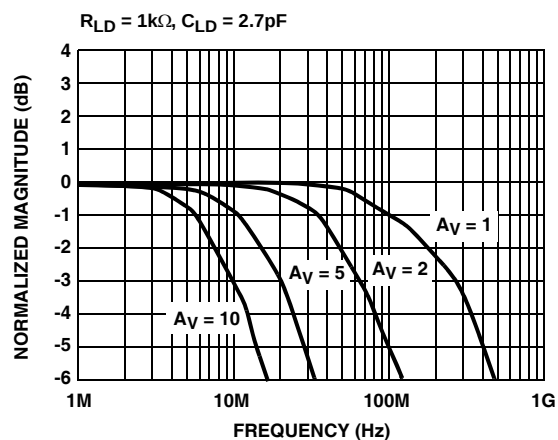


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS GAIN

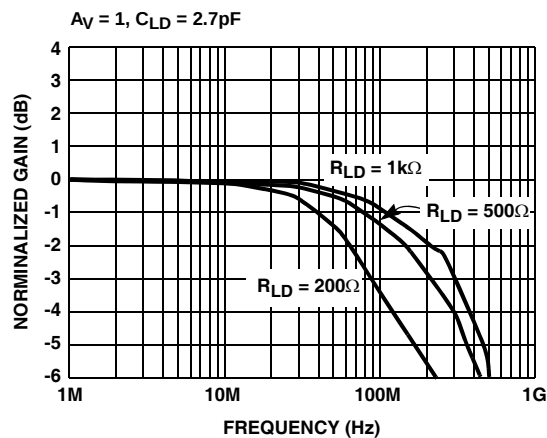
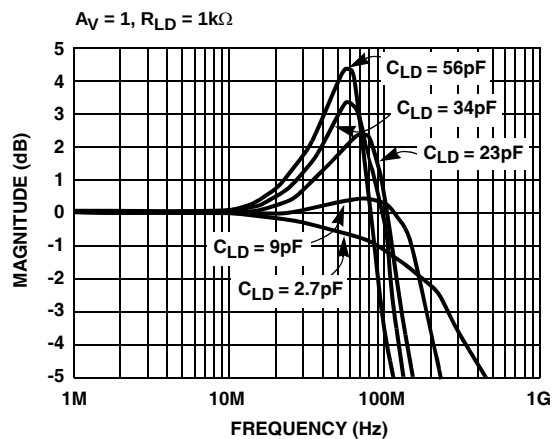
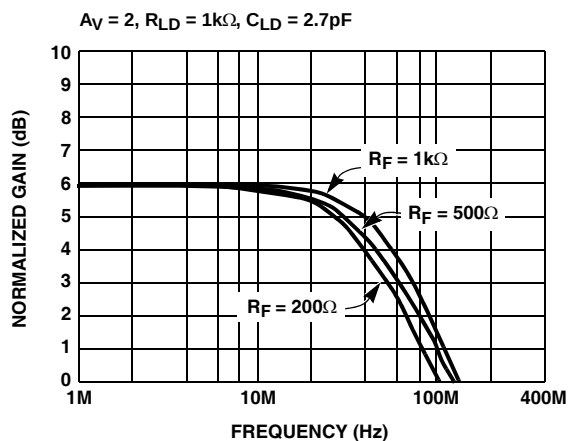
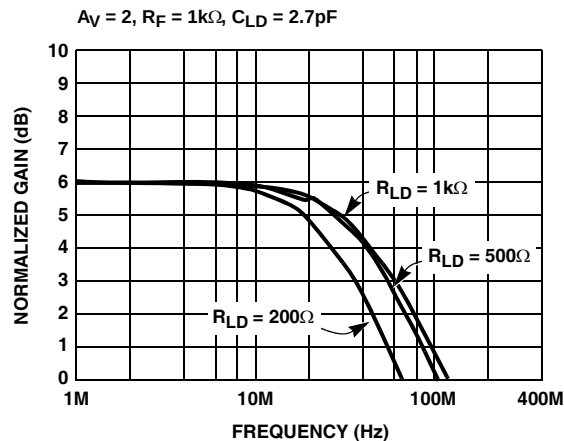
FIGURE 3. FREQUENCY RESPONSE vs R_{LD} FIGURE 4. FREQUENCY RESPONSE vs C_{LD} 

FIGURE 5. FREQUENCY RESPONSE

FIGURE 6. FREQUENCY RESPONSE vs R_{LD}

Typical Performance Curves (Continued)

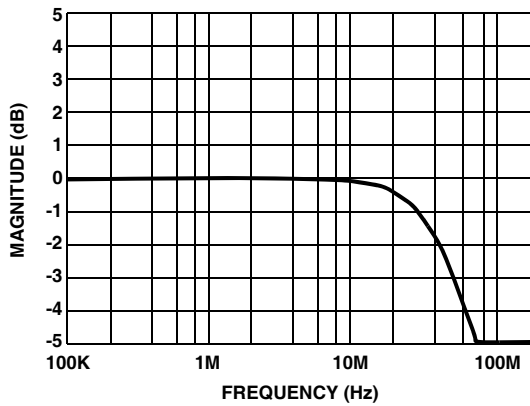


FIGURE 7. FREQUENCY RESPONSE - V_{REF}

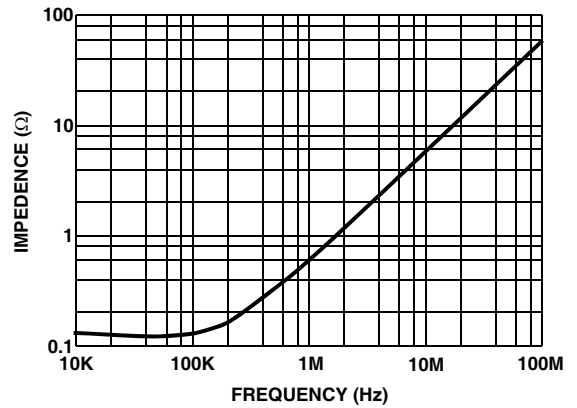


FIGURE 8. OUTPUT IMPEDANCE vs FREQUENCY

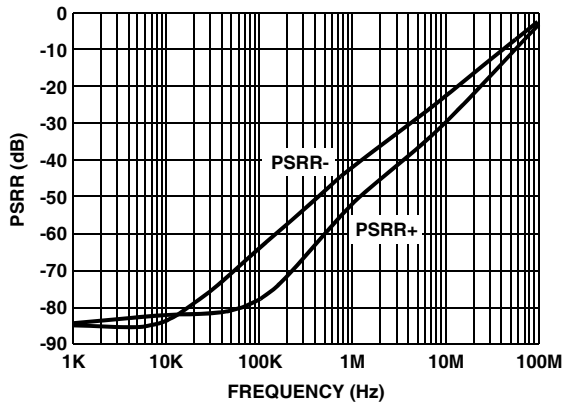


FIGURE 9. PSRR vs FREQUENCY

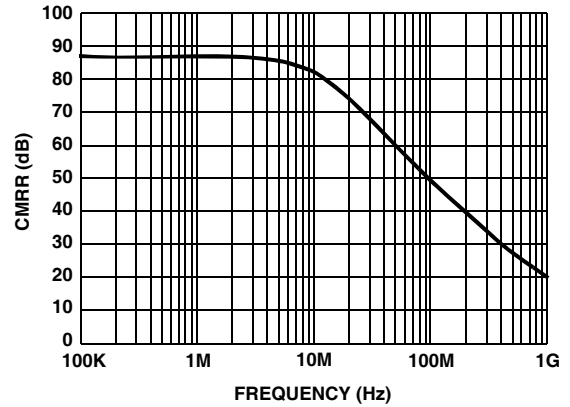


FIGURE 10. CMRR vs FREQUENCY

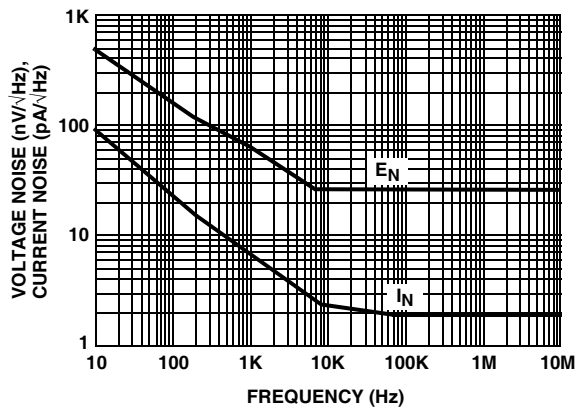


FIGURE 11. VOLTAGE AND CURRENT NOISE vs FREQUENCY

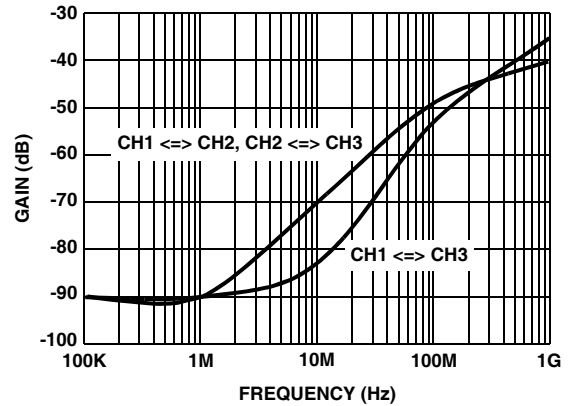


FIGURE 12. CHANNEL ISOLATION vs FREQUENCY

Typical Performance Curves (Continued)

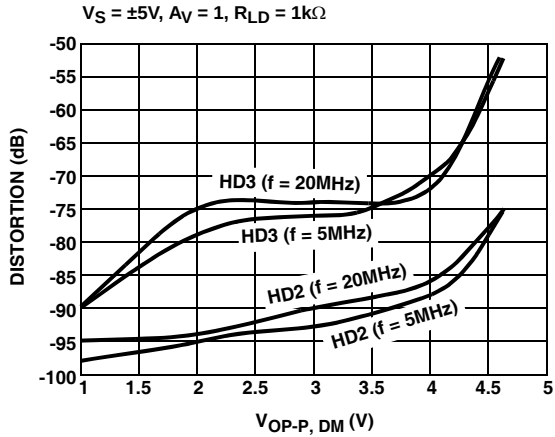


FIGURE 13. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

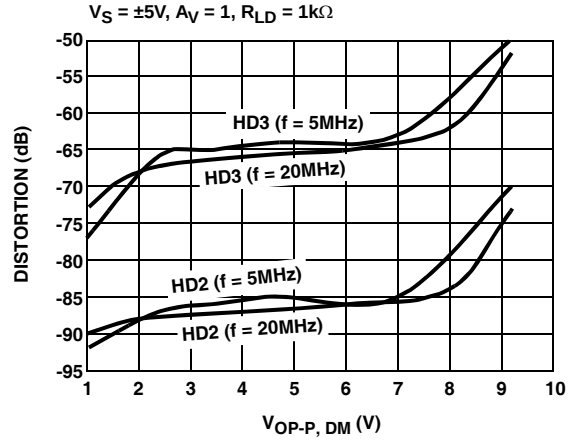


FIGURE 14. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

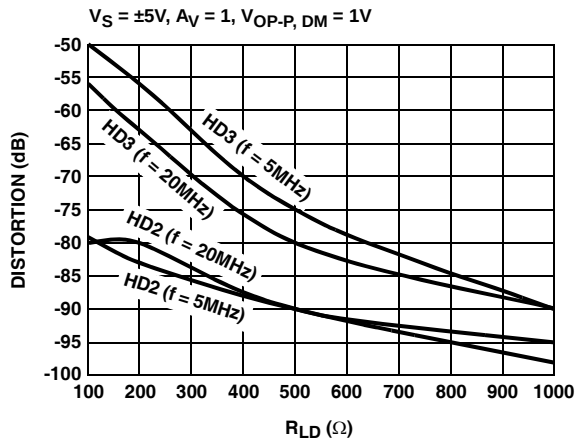


FIGURE 15. HARMONIC DISTORTION vs R_{LD}

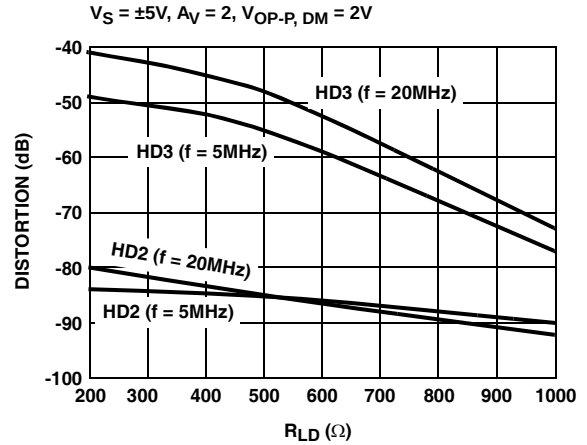


FIGURE 16. HARMONIC DISTORTION vs R_{LD}

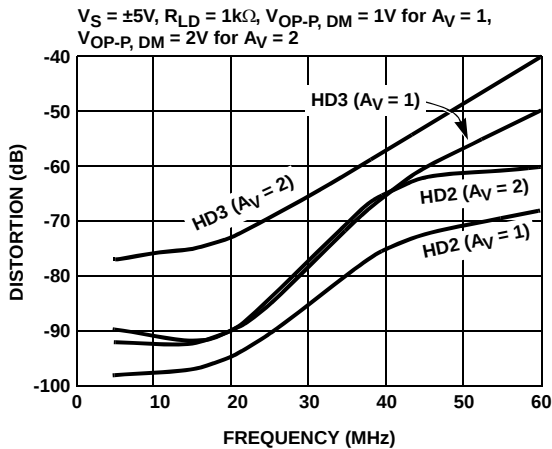


FIGURE 17. HARMONIC DISTORTION vs FREQUENCY

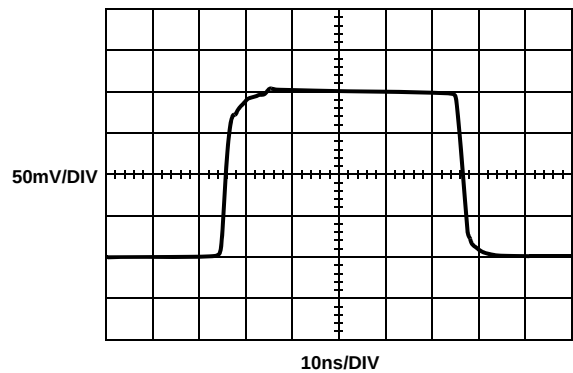


FIGURE 18. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

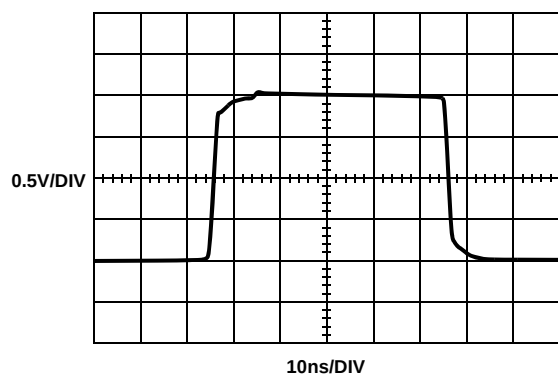


FIGURE 19. LARGE SIGNAL TRANSIENT RESPONSE

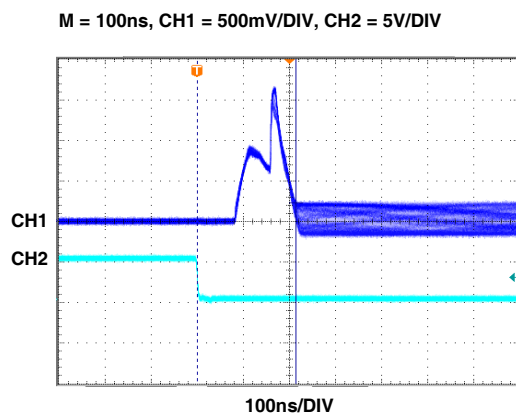


FIGURE 20. ENABLED RESPONSE

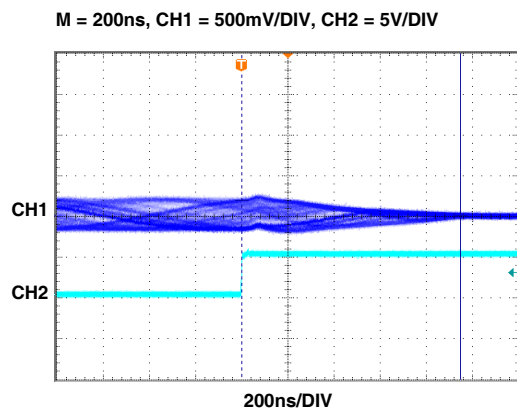


FIGURE 21. DISABLED RESPONSE

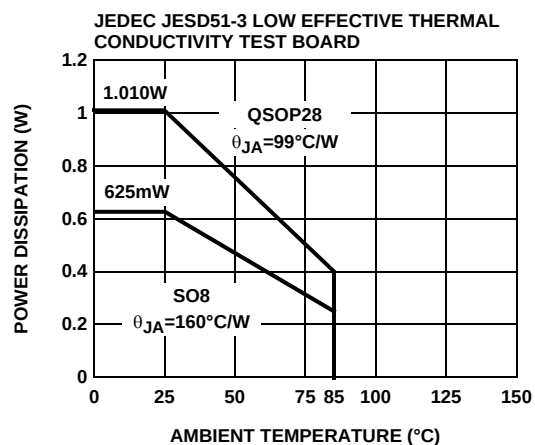


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

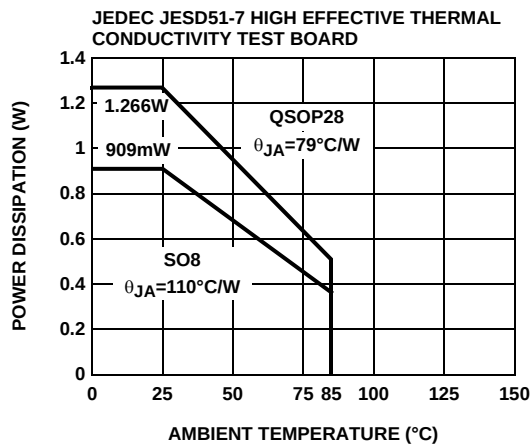
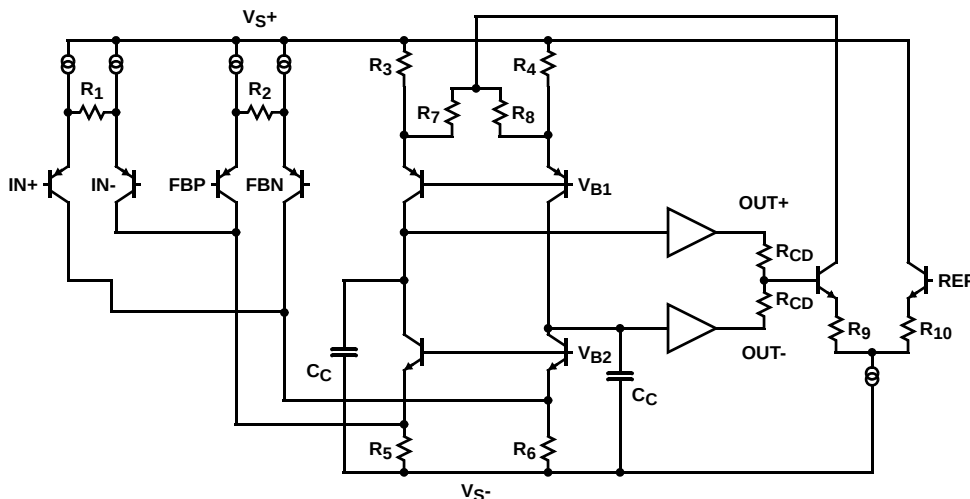


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5171 and EL5371 are wide bandwidth, low power and single ended to differential output amplifiers. The EL5171 is a single channel differential amplifier. Since the I_N^- pin and REF pin are tied together internally, the EL5171 can be used as a single ended to differential converter. The EL5371 is a triple channel differential amplifier. The EL5371 have a separate I_N^- pin and REF pin for each channel. It can be used as single/differential ended to differential converter. The EL5171 and EL5371 are internally compensated for closed loop gain of +1 or greater. Connected in gain of 1 and driving a $1k\Omega$ differential load, the EL5171 and EL5371 have a -3dB bandwidth of 250MHz. Driving a 200Ω differential load at gain of 2, the bandwidth is about 30MHz. The EL5371 is available with a power down feature to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The EL5171 and EL5371 have been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.5V to 3.4V for $\pm 5V$ supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.8V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal distorted.

The output of the EL5171 and EL5371 can swing from -3.9V to +3.9V at $1k\Omega$ differential load at $\pm 5V$ supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

For EL5171, since the I_N^- pin and REF pin are bounded together as the REF pin in an 8 Ld package, the signal at the REF pin is part of the common mode signal and also part of the differential mode signal. For the true balance differential outputs, the REF pin must be tied to the same bias level as the I_N^+ pin. For a $\pm 5V$ supply, just tie the REF pin to GND if the I_N^+ pin is biased at 0V with a 50Ω or 75Ω termination resistor. For a single supply application, if the I_N^+ is biased to half of the rail, the REF pin should be biased to half of the rail also.

The gain setting for EL5171 is:

$$V_{ODM} = V_{IN+} \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

$$V_{ODM} = V_{IN+} \times \left(1 + \frac{2R_F}{R_G} \right)$$

$$V_{OCM} = V_{REF} = 0V$$

Where:

- $V_{REF} = 0V$
- $R_{F1} = R_{F2} = R_F$

EL5371 has a separate I_N^- pin and REF pin. It can be used as a single/differential ended to differential converter. The voltage applied at REF pin can set the output common mode voltage and the gain is one.

The gain setting for EL5371 is:

$$V_{ODM} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

$$V_{ODM} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_F}{R_G} \right)$$

$$V_{OCM} = V_{REF}$$

Where:

- $R_{F1} = R_{F2} = R_F$

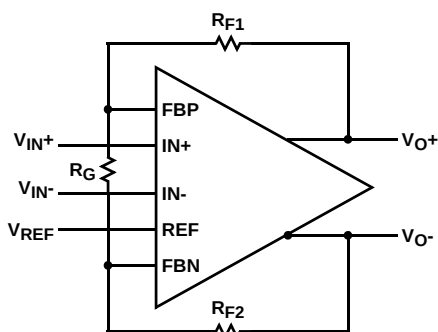


FIGURE 24.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the OUT+ pin to FBP pin and OUT- pin to FBN pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5171 and EL5371 depends on the load and the feedback network. R_F and R_G appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum bandwidth performance. For gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F between 500Ω to 1kΩ.

The EL5171 and EL5371 have a gain bandwidth product of 100MHz for $R_{LD} = 1k\Omega$. For gains ≥ 5 , its bandwidth can be predicted by the following equation:

$$\text{Gain} \times \text{BW} = 100\text{MHz}$$

Driving Capacitive Loads and Cables

The EL5171 and EL5371 can drive 50pF differential capacitor in parallel with 1kΩ differential load with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down (for EL5371 only)

The EL5371 can be disabled and placed its outputs in a high impedance state. The turn off time is about 0.95μs and the turn on time is about 215ns. When disabled, the amplifier's supply current is reduced to 1.7μA for I_{S+} and 120μA for I_{S-} typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_{S+} pin. Letting the $\overline{\text{EN}}$ pin float or applying a signal that is less than 1.5V below V_{S+} will enable the amplifier. The amplifier will be disabled when the signal at $\overline{\text{EN}}$ pin is above $V_{S+} - 0.5V$.

Output Drive Capability

The EL5171 and EL5371 have internal short circuit protection. Its typical short circuit current is ±90mA for EL5171 and ±70mA for EL5371. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL5171 and EL5371. It is possible to exceed the 135°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = i \times \left(V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}} \right)$$

Where:

- V_S = Total supply voltage
- I_{SMAX} = Maximum quiescent supply current per channel
- ΔV_O = Maximum differential output voltage of the application
- R_{LD} = Differential load resistance
- I_{LOAD} = Load current
- i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LD} to avoid the device overheat.

Typical Applications

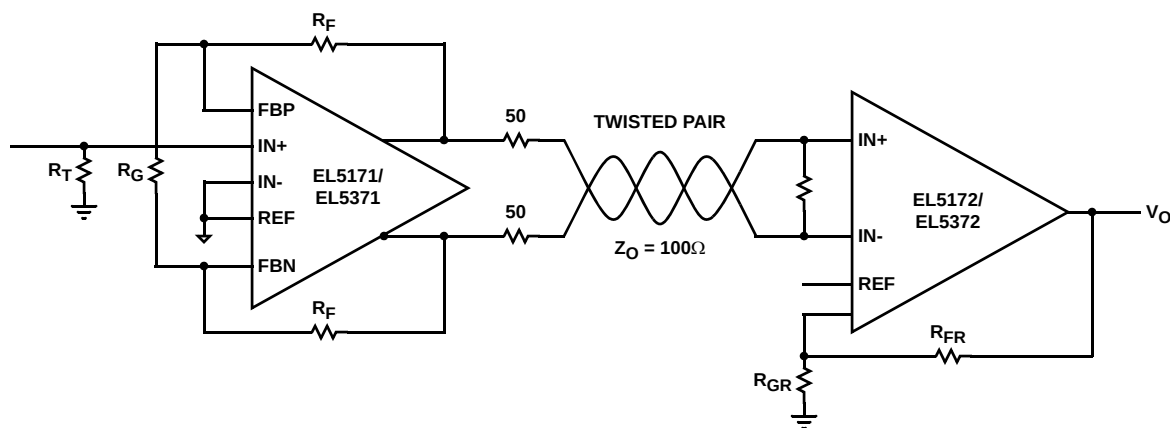


FIGURE 25. TWISTED PAIR CABLE RECEIVER

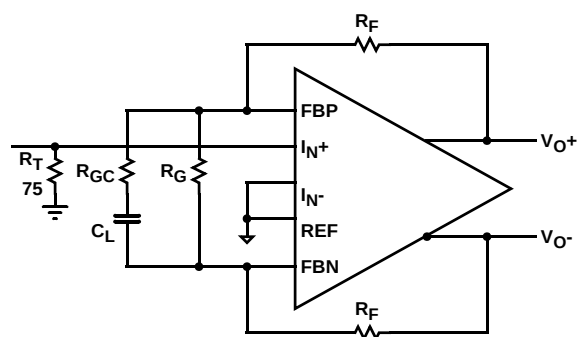
Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S - pin is connected to the ground plane, a single 4.7μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor from V_S + to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S - pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

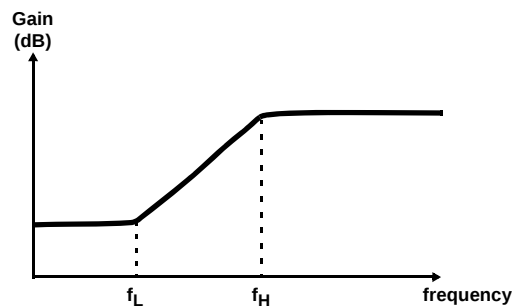
As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate

this loss is to boost the high frequency gain at the receiver side.



$$\text{DC Gain} = 1 + \frac{2R_F}{R_G}$$

$$(\text{HF})\text{Gain} = 1 + \frac{2R_F}{R_G \parallel R_{GC}}$$



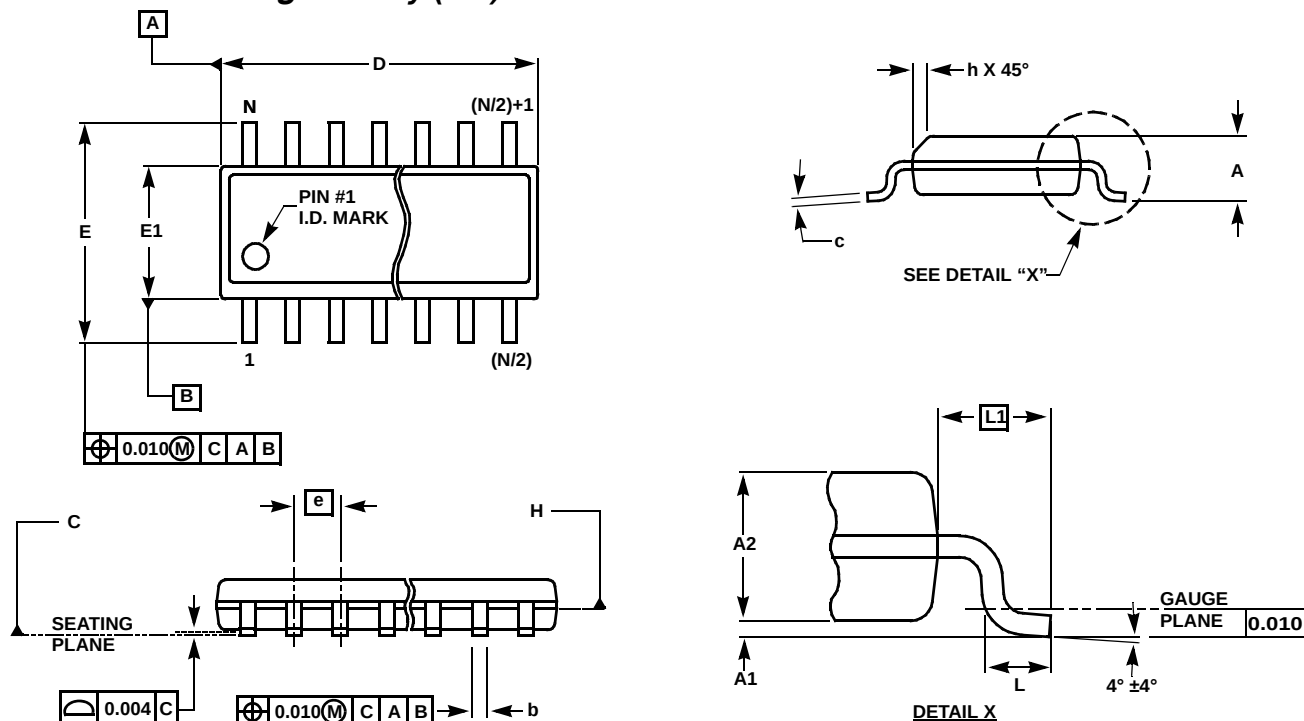
$$f_L \cong \frac{1}{2\pi R_G C_C}$$

$$f_H \cong \frac{1}{2\pi R_{GC} C_C}$$

FIGURE 26. TRANSMIT EQUALIZER

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

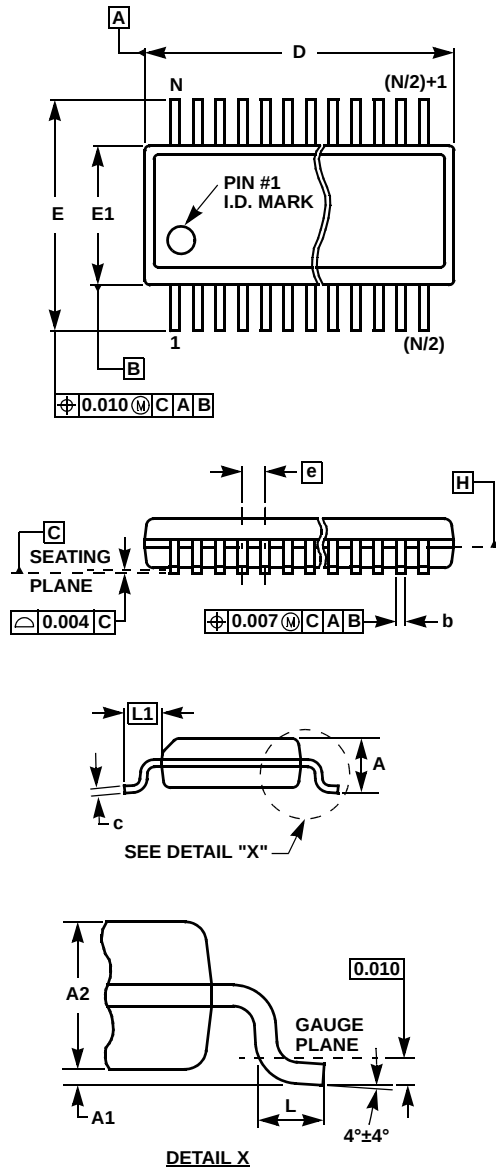
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	± 0.002	-
A2	0.056	0.056	0.056	± 0.004	-
b	0.010	0.010	0.010	± 0.002	-
c	0.008	0.008	0.008	± 0.001	-
D	0.193	0.341	0.390	± 0.004	1, 3
E	0.236	0.236	0.236	± 0.008	-
E1	0.154	0.154	0.154	± 0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	± 0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. E 3/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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