FNP300 I²C Interface Programming Manual

1 Scope

This document describes in detail the I²C communication interface of the FNP300 series. (FNP300-1012, FNP300-1024, FNP300-1048) This includes the physical layer and the SW protocol.

2 FNP300 I²C Interface General Characteristic

FNP300 I²C interface	**slave**
I²C Device Addressing Format	**7bit**
Device Address Range	**80_{Hex} ..$8F_{Hex}$**
Max. FNP300 on one I²C Bus	**8**
Maximum I²C clock	**100kHz**
Maximum I²C clock without holding the SCL line down	**8kHz**
Pull-Up Voltage	**3.3…4V**
SDA/SCL internal series resistors	**100Ω**
Internal Pull-Up	**--**
Internal Pull-Up voltage	**--**
Internal capacitance	**10pF**
Internal Pull-Up Address lines	**10kΩ**
Internal Pull-Up Address lines voltage	**3.3V**
Recommended external Pull-Up for SDA and SCL	**2.7kΩ …6.8kΩ**
Data Organization	**Serial EEPROM (128 x 8bit)**

Figure 2-1 Characteristic

3 Index

4 FNP300 I²C features

4.1 Dynamic data

The FNP300 series supports following monitoring features:

-Input Voltage in range/out of range
-Output Voltage in range/out of range
-Fan OK/failure
-Over Temperature true/false
-Power Supply seated/not seated
-Fan Speed [rpm]
-Inlet temperature [C°]

4.2 Static data

In the EEPROM are following static data stored:

-Power Supply Model
-Serial Number
-Power-One Revision
-MFG Year
-MFG Month
-MFG Day
-MFG Name
-MFG Location Code
-Specified Output Voltage
-Specified Output Current
-Specified Output Power
-Minimum Specified Input Voltage
-Maximum Specified Input Voltage
-Checksum over static range
-68 Bytes EEPROM for Customer use

5 General I²C HW configuration

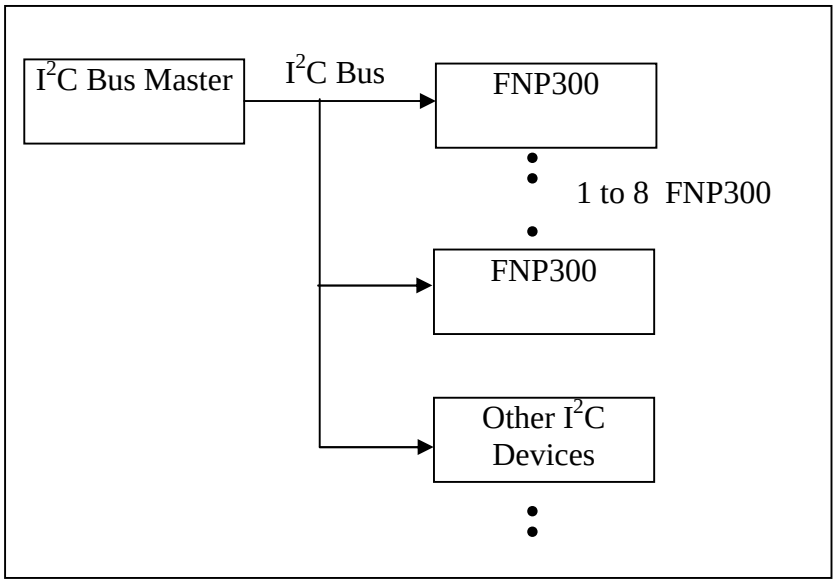


Figure 5-1 System Overview

5.1 Connecting the FNP300 to the I²C Bus

The following diagram shows how the FNP300 can be connected to the I²C Bus.

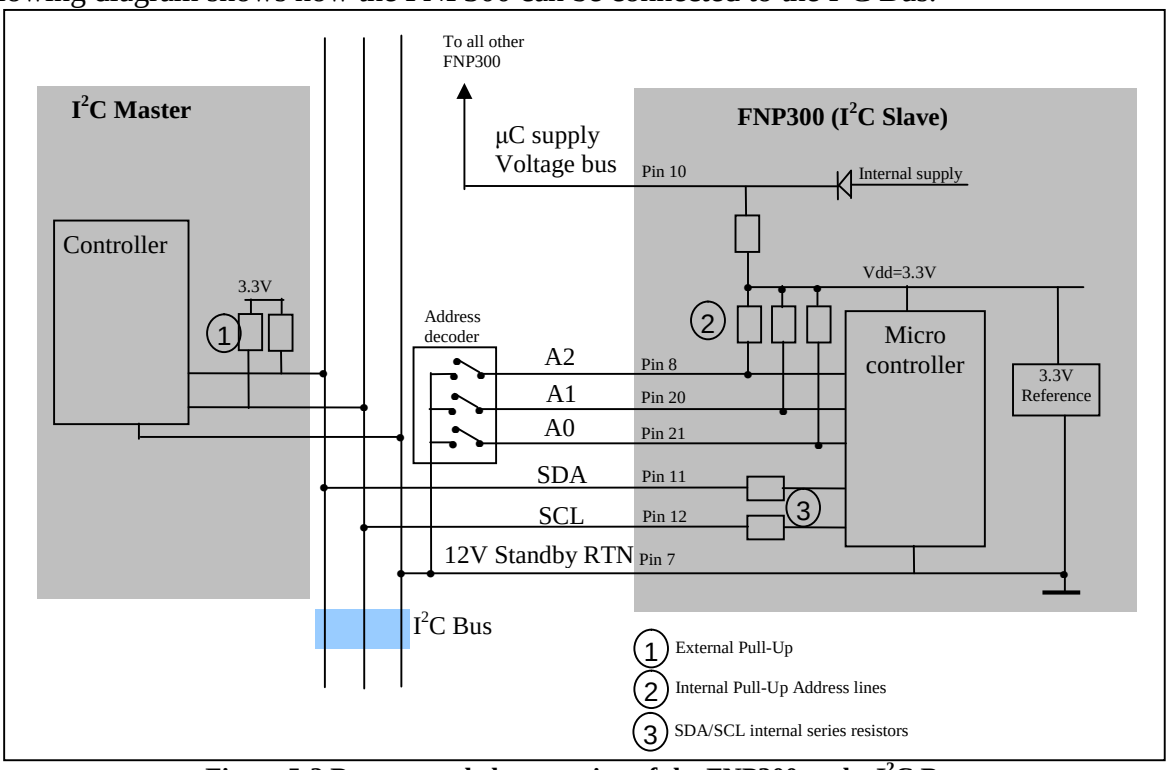


Figure 5-2 Recommended connecting of the FNP300 to the I²C Bus

5.2 FNP300 I²C Supply (Slave)

The FNP300 Micro Controller is powered over the internal supply of the FNP 300. For redundancy in case of AC failure or FNP300 internal failure the FNP 300 Micro Controller can be powered over the "µC supply Voltage bus" (pin 10; 5 to 7V). If there is no power for the FNP300 Micro Controller the entire I²C Bus is blocked.

5.3 Device Address

The first byte after the START condition on the Bus is the device address sent out by the Bus Master to determine which device is being selected. The I²C Bus allows 7-bit or 10-bit addressing. The FNP300 Interface uses a 7-bit address mode as defined in the Philips I²C specification. Each FNP300 device has to be assigned to a unique address.

As shown below in Figure 5-3 Device Address the address byte is built up from three parts:
- Bit 4...7: These bits are always the same independent of any address line.
- Bit 1...3: These bits depends how the Address line A0...A2 is connected on the backplane on the address decoder. These are logic 1 if open and logic 0 if wired to 0V (12V Standby RTN).
-Bit 0: This bit is the read/write bit (R=1/W=0) and determines the direction of the data from or to the Master.

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
FNP300 Device Address	1	0	0	0	addr. line A2	addr. line A1	addr. line A0	direc.
	fix	fix	fix	fix	A2	A1	A0	R/W

Figure 5-3 Device Address

	Address Line A2	Address Line A1	Address Line A0	Read/ Write	Device Address [Bin]	Device Address [Hex]	Device Address [Dec]
FNP300 Device address	open	open	open	read	1000'1111	8F	143
FNP300 Device address	open	open	open	write	1000'1110	8E	142
FNP300 Device address	open	open	0V	read	1000'1101	8D	141
FNP300 Device address	open	open	0V	write	1000'1100	8C	140
FNP300 Device address	open	0V	open	read	1000'1011	8B	139
FNP300 Device address	open	0V	open	write	1000'1010	8A	138
FNP300 Device address	open	0V	0V	read	1000'1001	89	137
FNP300 Device address	open	0V	0V	write	1000'1000	88	136
FNP300 Device address	0V	open	open	read	1000'0111	87	135
FNP300 Device address	0V	open	open	write	1000'0110	86	134
FNP300 Device address	0V	open	0V	read	1000'0101	85	133
FNP300 Device address	0V	open	0V	write	1000'0100	84	132
FNP300 Device address	0V	0V	open	read	1000'0011	83	131
FNP300 Device address	0V	0V	open	write	1000'0010	82	130
FNP300 Device address	0V	0V	0V	read	1000'0001	81	129
FNP300 Device address	0V	0V	0V	write	1000'0000	80	128

Figure 5-4 Device Address Table

Example: On the backplane A2 and A0 are connected to 0V and A1 left open, you will have the following device address to read a byte from the FNP:

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
FNP300 Device Address	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**
	fix	fix	fix	fix	A2	A1	A0	R

->$10000101_{Bin}=85_{Hex}=133_{Dec}$

5.4 I²C Bus Master and clock (SCL) speed

The I²C Bus Master controls communications between the Master and all I²C devices connected to the bus. If during an I²C communication cycle the FNP300 is interrupted by an internal service interrupt, the FNP300 will hold the SCL line low to force the master into a wait state. Data transfer will continue when the FNP300 releases the SCL line.
Please note if the I²C bus is communicating with a clock frequency slower than 8 kHz, the SCL line will not be held low.

5.5 Maximum and minimum values for Pull-Up resisters

For I²C-bus systems, the values of the Pull-Up resistors depend on the following parameters:
- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of the Pull-Up resistor due to the specified minimum sink current of 3mA. On a 3.3V supply, this makes $\mathbf{R_{min}=3.3V/3mA=1.1k\Omega}$.
The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of the Pull-Up resister due to the specified rise time. For a System with 120pF capacitance (two FNP300 and a wire capacitance of 100pf) $\mathbf{R_{max}=8k\Omega}$.

For further information concerning the Pull-Up resister, refer to:
I²C Bus specification, 16.1 Maximum and minimum values of resistors Rp and Rs for Standard-mode I2C-bus devices.

6 SW Protocol

The data are organized like a serial I^2C EEPROM. Therefore each EEPROM address has defined data; this definition is documented in the file: FNP300-xxxxEEPROM_xx.pdf

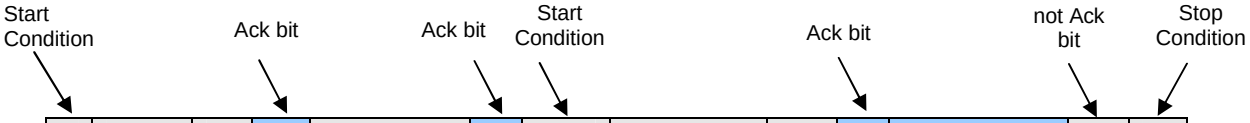
	Dez		Hex
Address	0	static data	0
	1	static data	1
	53	static data	35
	54	static data	36
	55	checksum over static data	37
	56	dynamic data	38
	57	dynamic data	39
	58	dynamic data	3A
	59	open for customer use	3B
	60	open for customer use	3C
	125	open for customer use	7D
	126	open for customer use	7C
	127	reserved	7E

Figure 6-1: Data Organization

There are three different message formats implemented in the FNP300:
-Read a byte
-Read a block
-Write a byte

6.1 How to Read a byte

1) "Start condition" from Master
2) Master sends "Device address" with "write attribute"
3) "Acknowledge" from Slave device (FNP300)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP300)
6) "Repeated start" from Master (Sr/S)
7) Master sends "Device address" with "read attribute"
8) "Acknowledge" from Slave device (FNP300)
9) Slave sends "Data byte"
10) "Not Acknowledge" from Master (power management system)
11) "Stop condition" from Master



S	Slave Adr.	W	A	EEPROM Adr.	A	Sr/S	Slave Adr.	R	A	Data Byte	/A	P
	8bit			8 bit			8bit			8 bit		

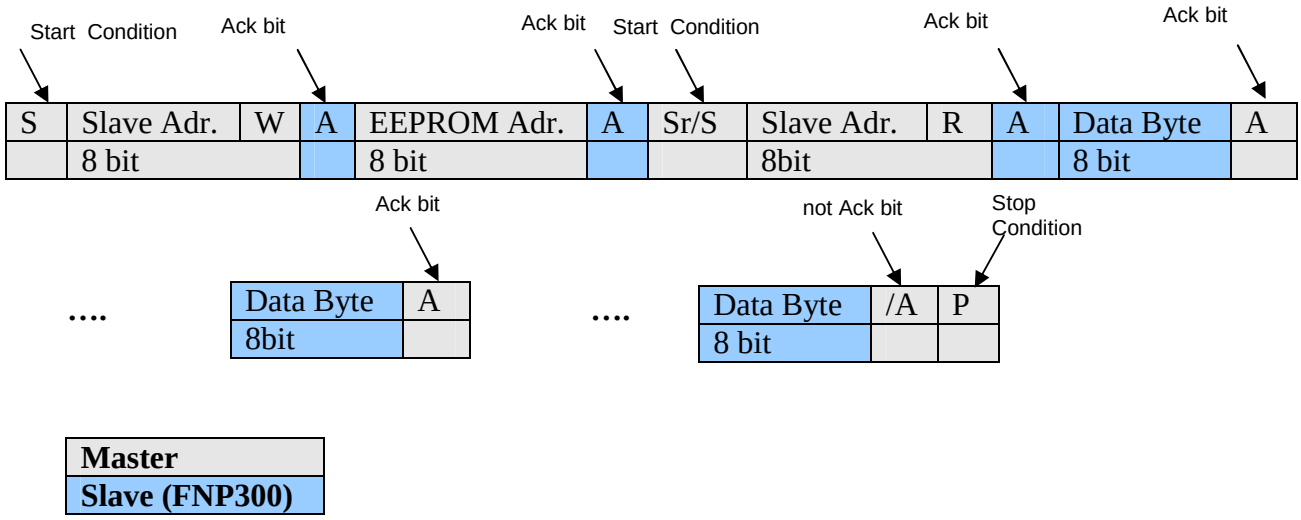
Master
Slave (FNP300)

6.2 How to read a block

1) "Start condition" from Master
2) Master sends "Device address" with "write attribute"
3) "Acknowledge" from Slave device (FNP300)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP300)
6) "Repeated start" from Master (Sr/S)
7) Master sends "Slave address" with "read attribute"
8) "Acknowledge" from Slave device (FNP300)
9) Slave sends "Data byte"
10) "Acknowledge" from Master (power management system)

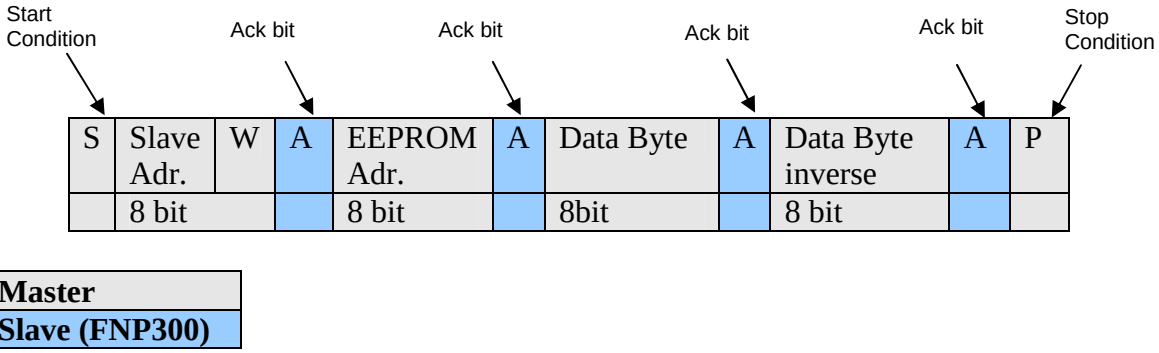
n-time repetition of step 9) and 10)

11) Slave sends "Data byte"
12) "Not Acknowledge" from Master (power management system)
13) "Stop condition" from Master



6.3 How to write a byte

1) "Start condition" from Master
2) Master sends "Slave address" with "write attribute"
3) "Acknowledge" from Slave device (FNP300)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP300)
6) Master sends "Data byte"
7) "Acknowledge" from Slave device (FNP300)
8) Master sends "Inversed Data byte " (same data just inverse sent)
9) "Acknowledge" from Slave device (FNP300)
10) "Stop condition" from Master



Note: "inverse" means bit inverse.

Example

	Value [Bin]	Value [Hex]	Value [Dec]
Data	**1010'1010**	AA	170
Data Inverse	**0101'0101**	55	85

Figure 6-2: Bit Inverse

7 Power-One I²C Interface tool

The Power-One I²C – Management Software (HZZ02002SW, www.power-one.com) demonstrates all the I²C interface features of the FNP300.

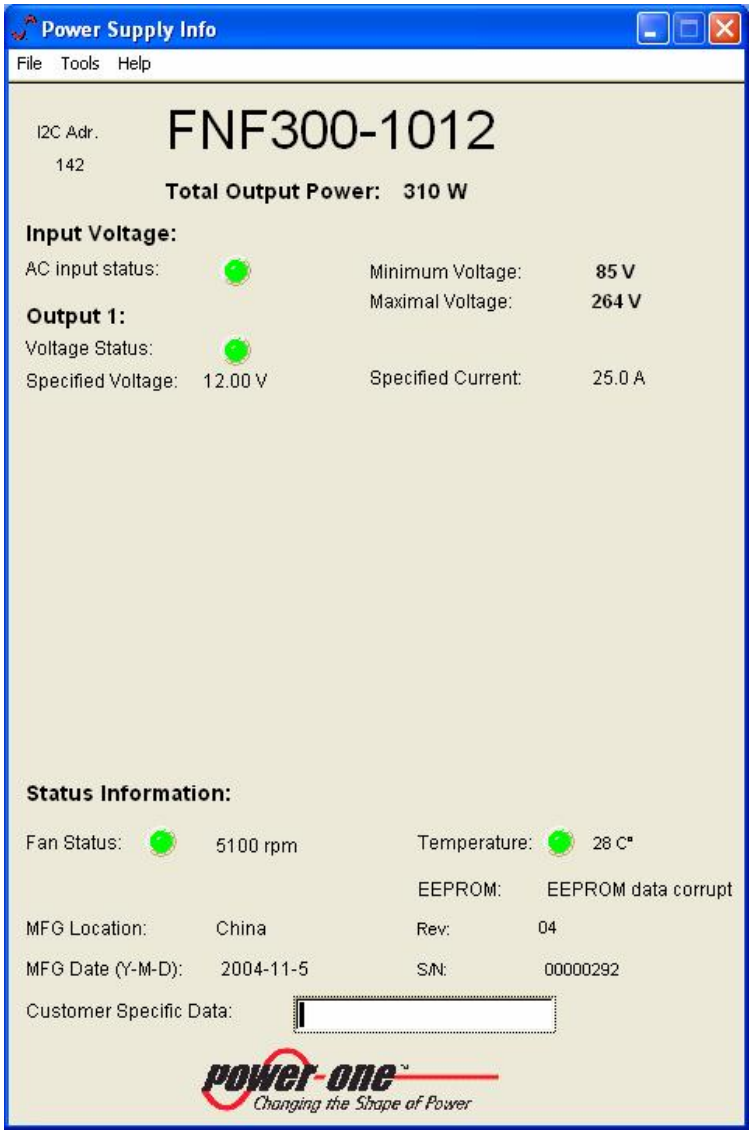
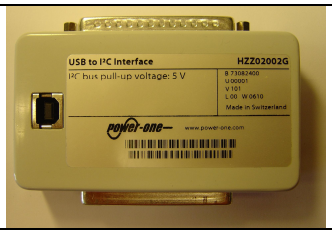


Figure 7-1 Screenshot FNP300

Power-One I²C – Management Software supports two I²C converters:

iPort MIIC-201 (Micro Computer Control)	HZZ02002G from Power-One
	

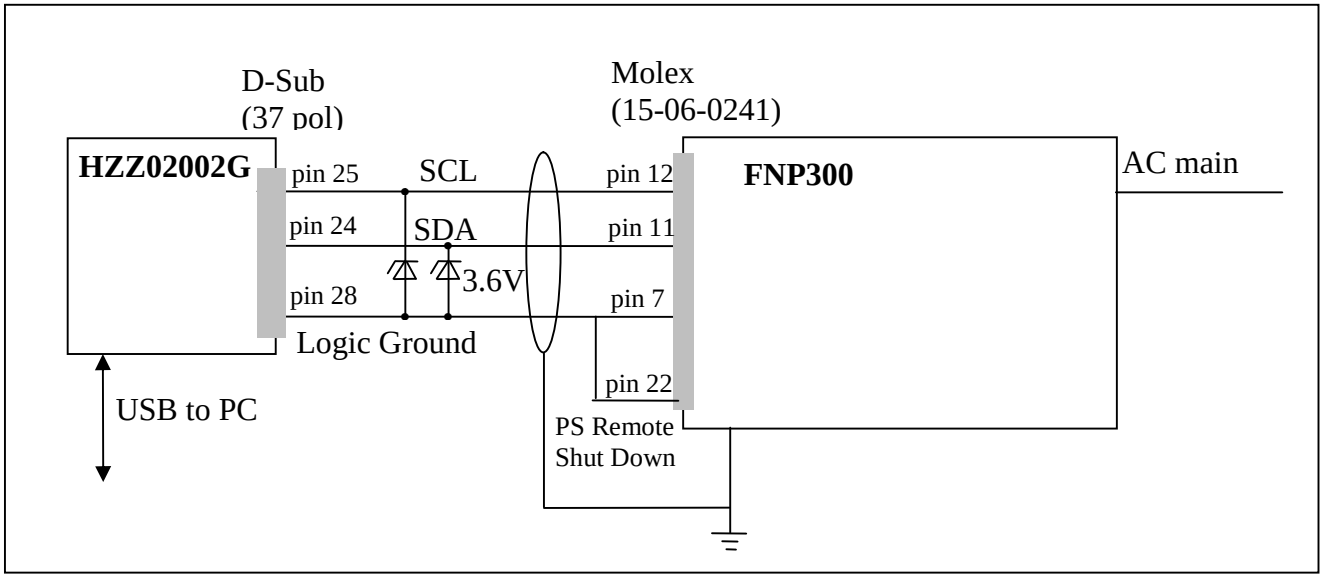


Figure 7-2 HZZ02002G to FNP300 cable

The HZZ02002G has the Pull-Up resisters connected to 5V and 3.3V compatible inputs. Please clamp the SCL and SDA lines to 3.6V with Z-Diodes. Connect “SDA”(pin 11), “SCL”(pin 12) and “12V Standby RTN”(pin 7) to the I^2C to RS232/USB converter. Connect “PS Remote Shut Down” to “Vo2 RTN” to enable the FNP300 and plug the FNP300 to the Mains.

The I^2C device address will be $8E_{Hex}$ (/write) and $8F_{Hex}$ (read).

In your final application the I^2C master will be a Micro Computer or an FPGA with an I^2C interface. That makes it easy and inexpensive to use the interface.

8 Bibliography

-Philips Semiconductors, The I 2C-BUS Specification, V.2.1, Document order number: 9398 393 40011
www.semiconductors.**philips**.com/ acrobat/literature/9398/39340011.pdf

-Philips SemiconductorsI2C Handbook
www.semiconductors.**philips**.com/ acrobat/various/**philips_i2c**_handbook.pdf

-Power-One, FNP300 Data-Sheet
-Power-One, FNP300 EEPROM Table

9 Figure Index

10 Glossary

µC	Micro Controller
Bin	Value in binary number system
Dec	Value in decimal number system
EEPROM	Electrically Erasable Programmable Read Only Memory
Hex	Value in hexadecimal number system
I²C Bus	Inter-Integrated Circuit Bus
kHz	SI unit of frequency: Hertz(1/s) * 10^3
LSB	Least significant bit
MFG	Manufacturing
MSB	Most significant bit
pF	SI unit of Capacitance: farad($kg^{-1}\cdot m^{-2}\cdot A^2\cdot s4$) * 10^{-12}
SCL	serial clock line
SDA	serial data line