

# FDME820NZT

## N-Channel PowerTrench® MOSFET

20 V, 9 A, 18 mΩ

### Features

- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 9$  A
- Max  $r_{DS(on)}$  = 24 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 7.5$  A
- Max  $r_{DS(on)}$  = 32 mΩ at  $V_{GS} = 1.8$  V,  $I_D = 7$  A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 Thin
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level >2.5 kV (Note3)
- RoHS Compliant

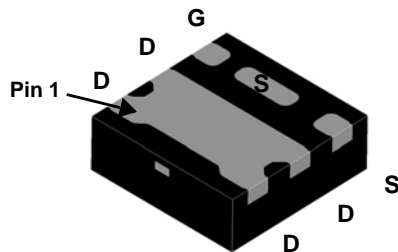


### General Description

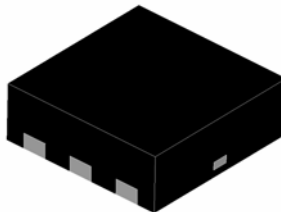
This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the  $r_{DS(ON)}$  @  $V_{GS} = 1.8$  V on special MicroFET leadframe.

### Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion

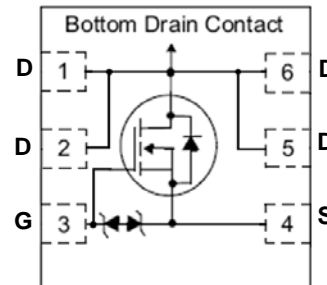


BOTTOM



TOP

MicroFET 1.6x1.6 Thin



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current -Continuous $T_A = 25$ °C (Note 1a)	9	A
	-Pulsed	40	
$P_D$	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1a)	2.1	W
	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	70	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	190	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8T	FDME820NZT	MicroFET 1.6x1.6 Thin	7"	8 mm	5000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		20		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	0.5	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		14	18	m $\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 7.5\text{ A}$		17	24	
		$V_{GS} = 1.8\text{ V}, I_D = 7\text{ A}$		26	32	
		$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}, T_J = 125\text{ }^\circ\text{C}$		19	24	

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		865		pF
$C_{oss}$	Output Capacitance			203		pF
$C_{rss}$	Reverse Transfer Capacitance			190		pF
$R_g$	Gate Resistance			1.0		$\Omega$

### Switching Characteristics

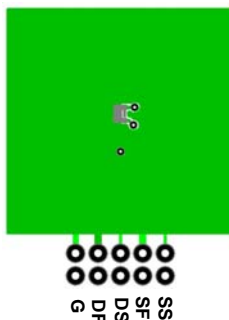
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 4\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 2\text{ }\Omega$		9		ns
$t_r$	Rise Time			5		ns
$t_{d(off)}$	Turn-Off Delay Time			19		ns
$t_f$	Fall Time			5		ns
$Q_g$	Total Gate Charge		$V_{DD} = 4.2\text{ V}, I_D = 3\text{ A}, V_{GS} = 4.3\text{ V}$		8.0	
$Q_g$	Total Gate Charge	$V_{DD} = 4.2\text{ V}, I_D = 3\text{ A}, V_{GS} = 4.5\text{ V}$		8.5		nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 10\text{ V}, I_D = 9\text{ A}$		1.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.2		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.6\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 9\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 9\text{ A}, di/dt = 100\text{ A/us}$		18		ns
$Q_{rr}$	Reverse Recovery Charge			4		nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $70\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.

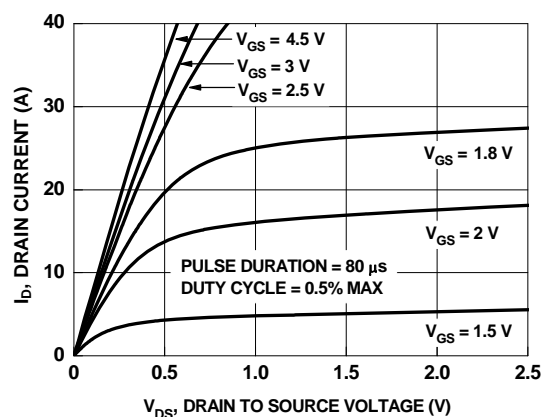


b.  $190\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

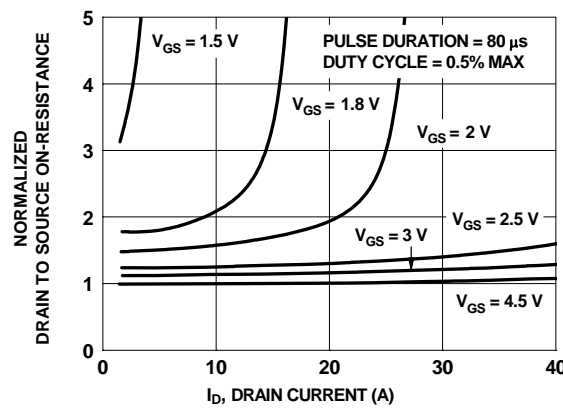
2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

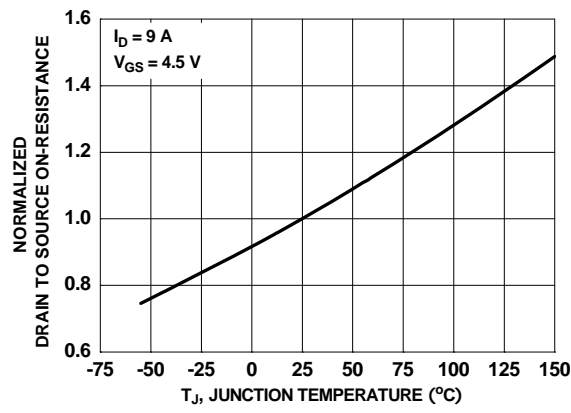
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



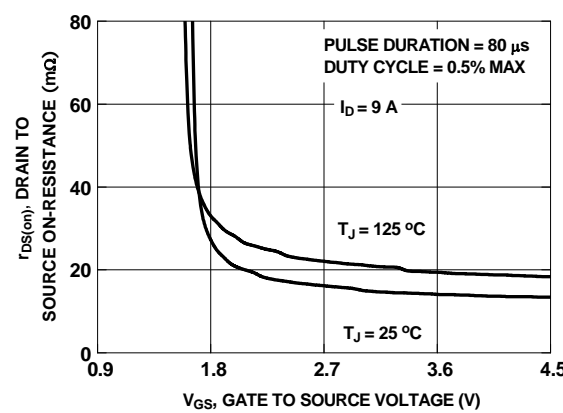
**Figure 1. On Region Characteristics**



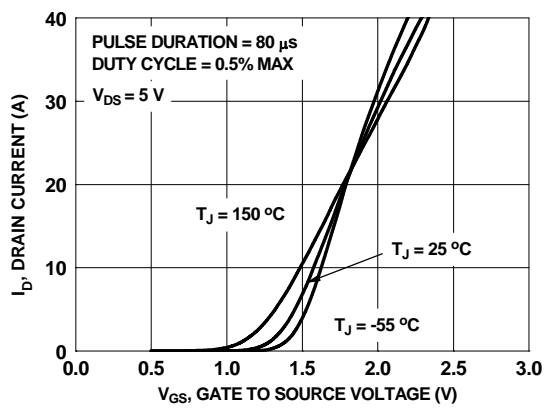
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



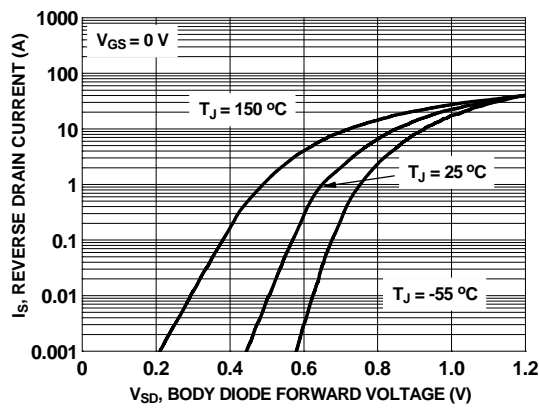
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

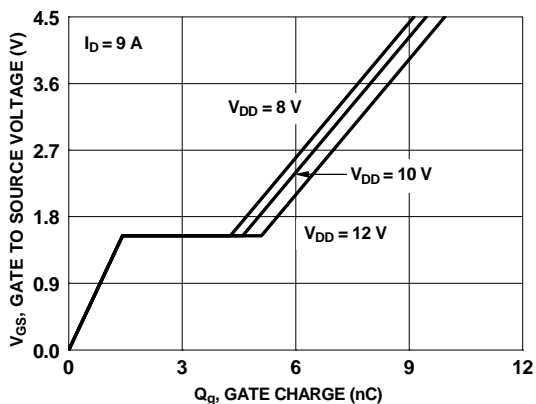


**Figure 5. Transfer Characteristics**

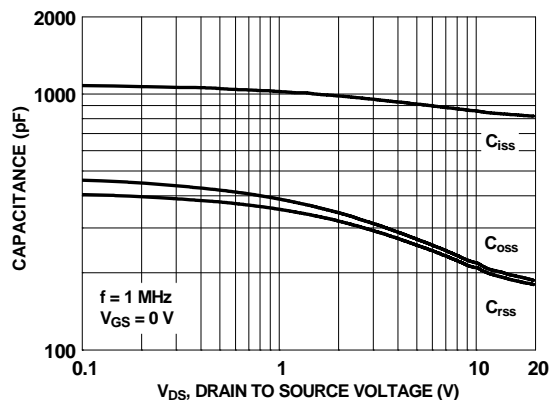


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

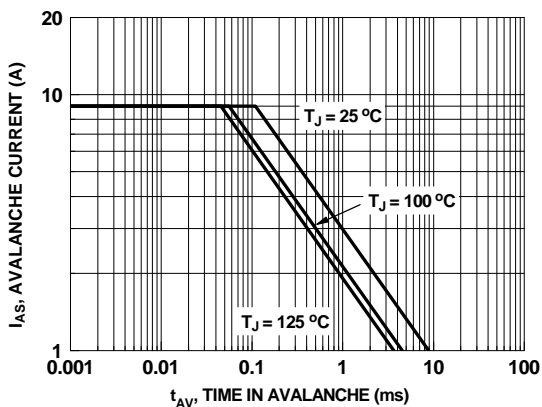
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



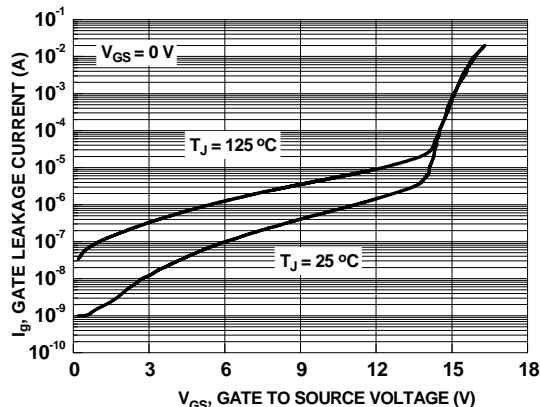
**Figure 7. Gate Charge Characteristics**



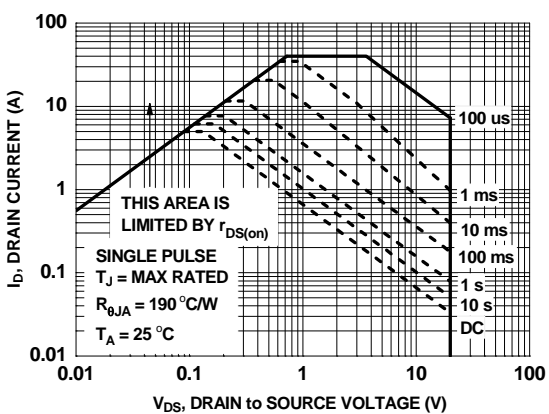
**Figure 8. Capacitance vs Drain to Source Voltage**



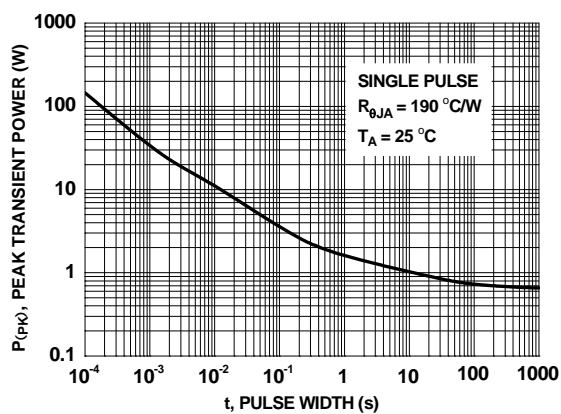
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

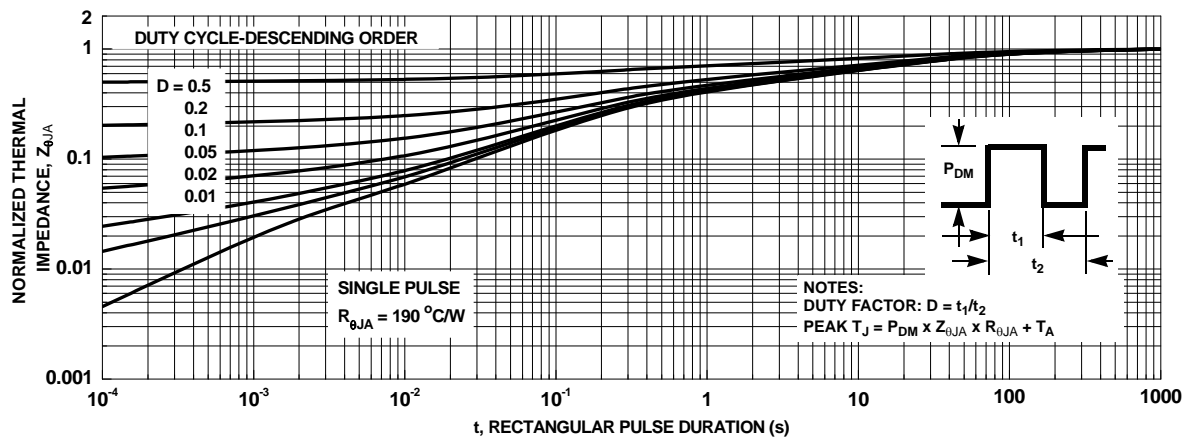


**Figure 11. Forward Bias Safe Operating Area**



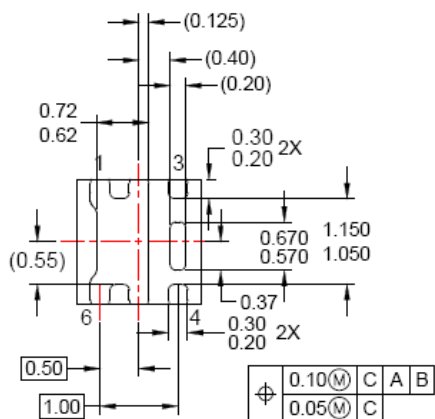
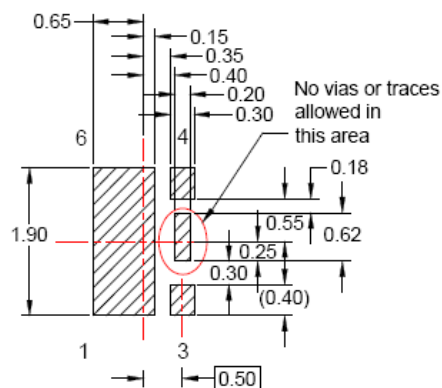
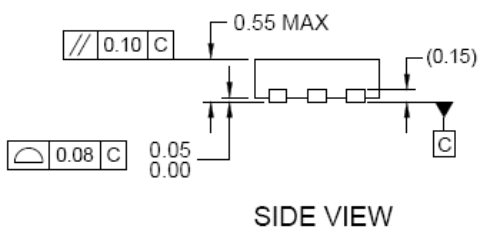
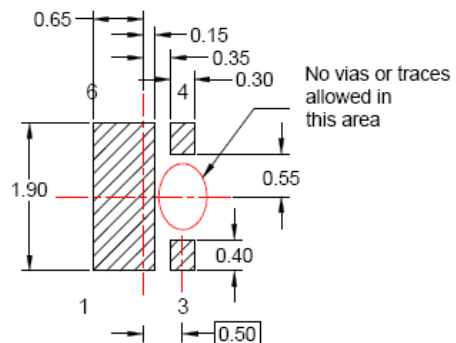
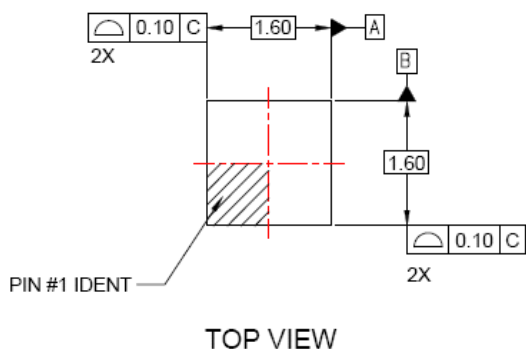
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout




- NOTES:
- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  - D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY



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| Build it Now™   | GreenBridge™                                    | QFET®                                 | TinyBuck®        |
| CorePLUSTM  | Green FPS™                                      | QS™                                   | TinyCalc™        |
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| ESBC™   | MicroFET™                                       | STEALTH™                              | μSerDes™         |
|  | MicroPak™                                       | SuperFET®                             | UHC®             |
| Fairchild®  | MicroPak2™                                      | SuperSOT™-3                           | Ultra FRFET™     |
| Fairchild Semiconductor®  | MillerDrive™                                    | SuperSOT™-6                           | UniFET™          |
| FACT Quiet Series™  | MotionMax™                                      | SuperSOT™-8                           | VCX™             |
| FACT®   | mWSaver®  | SupreMOS®                             | VisualMax™       |
| FAST®   | OptoHi™   | SyncFET™                              | VoltagePlus™     |
| FastvCore™  | OPTOLOGIC®                                      |                                       | XS™              |
| FETBench™   | OPTOPLANAR®                                     |                                       |                  |
| FPS™  |   |                                       |                  |

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**Definition of Terms**

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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