

FEATURES

- 1.5 Ω on resistance
- 0.3 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Continuous current per channel
 - LFCSP package: 250 mA
 - TSSOP package: 190 mA
- Fully specified at $+12$ V, ± 15 V, and ± 5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 16-lead, 4 mm $\times$ 4 mm LFCSP

APPLICATIONS

- Automated test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communications systems
- Relay replacement

GENERAL DESCRIPTION

The ADG1411/ADG1412/ADG1413 are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS[®] process. *i*CMOS (industrial CMOS) is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching signals.

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG1411/ADG1412/ADG1413 contain four independent single-pole/single-throw (SPST) switches. The ADG1411 and

FUNCTIONAL BLOCK DIAGRAM

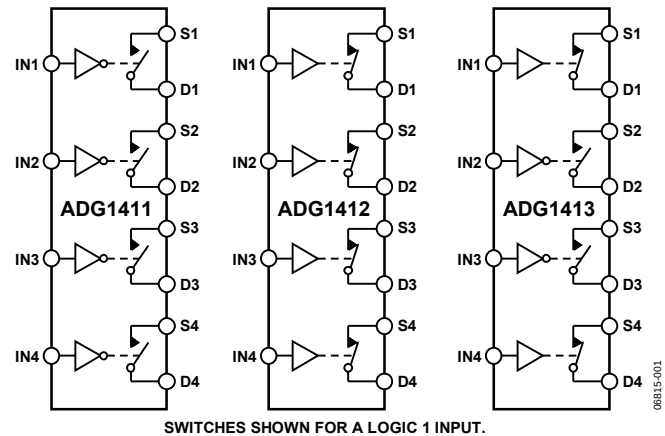


Figure 1.

ADG1412 differ only in that the digital control logic is inverted. The ADG1411 switches are turned on with Logic 0 on the appropriate control input, whereas the ADG1412 switches are turned on with Logic 1. The ADG1413 has two switches with digital control logic similar to that of the ADG1411; the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG1413 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection, which results in minimum transients when the digital inputs are switched.

PRODUCT HIGHLIGHTS

1. 2.6 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: $<0.03 \mu\text{W}$.
4. 16-lead TSSOP and 16-lead, 4 mm $\times$ 4 mm LFCSP packages.

Rev. A

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REVISION HISTORY

3/09—Rev. 0 to Rev. A	
Changes to Power Requirements, I _{DD} , Digital Inputs = 5 V	
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Changes to Power Requirements, I _{DD} , Digital Inputs = 5 V	
Parameter Table 2	4
5/08—Revision 0: Initial Version	

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance, R _{ON}	1.5	2.3	2.6	Ω typ	V _S = ±10 V, I _S = −10 mA; see Figure 23
	1.8			Ω max	V _{DD} = +13.5 V, V _{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR _{ON}	0.1			Ω typ	V _S = ±10 V , I _S = −10 mA
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness, R _{FLAT(ON)}	0.3			Ω typ	V _S = ±10 V, I _S = −10 mA
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.03			nA typ	V _{DD} = +16.5 V, V _{SS} = −16.5 V
	±0.55	±2	±12.5	nA max	V _S = ±10 V, V _D = ∓10 V; see Figure 24
Drain Off Leakage, I _D (Off)	±0.03			nA typ	V _S = ±10 V, V _D = ∓10 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I _D , I _S (On)	±0.15			nA typ	V _S = V _D = ±10 V; see Figure 25
	±2	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.005		±0.1	μA typ	V _{IN} = V _{GND} Or V _{DD}
				μA max	
Digital Input Capacitance, C _{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t _{ON}	100	170	190	ns typ	R _L = 300 Ω, C _L = 35 pF
	150			ns max	V _S = 10 V; see Figure 30
t _{OFF}	90	140	160	ns typ	R _L = 300 Ω, C _L = 35 pF
	120			ns max	V _S = 10 V; see Figure 30
Break-Before-Make Time Delay, t _D (ADG1413 Only)	25			ns typ	R _L = 300 Ω, C _L = 35 pF
			10	ns min	V _{S1} = V _{S2} = 10 V; see Figure 31
Charge Injection, Q _{INJ}	−20			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 32
Off Isolation	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−100			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.014			% typ	R _L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	170			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
Insertion Loss	−0.35			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
C _S (Off)	23			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	23			pF typ	V _S = 0 V, f = 1 MHz
C _D , C _S (On)	116			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1	μA typ	V _{DD} = +16.5 V, V _{SS} = −16.5 V
				μA max	Digital inputs = 0 V or V _{DD}
I _{DD}	220		380	μA typ	Digital inputs = 5 V
				μA max	
I _{SS}	0.001		1	μA typ	Digital inputs = 0 V or V _{DD}
				μA max	
V _{DD} /V _{SS}			±4.5/±16.5	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

ADG1411/ADG1412/ADG1413

+12 V SINGLE SUPPLY

$V_{DD} = 12 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	2.8 3.5	4.3	4.8	Ω typ Ω max	$V_S = 0 \text{ V}$ to 10 V, $I_S = -10 \text{ mA}$; see Figure 23 $V_{DD} = 10.8 \text{ V}$, $V_{SS} = 0 \text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.13			Ω typ	$V_S = 0 \text{ V}$ to 10 V, $I_S = -10 \text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.21 0.6 1.1	0.23	0.25 1.3	Ω max Ω typ Ω max	$V_S = 0 \text{ V}$ to 10 V, $I_S = -10 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02 ± 0.55	± 2	± 12.5	nA typ nA max	$V_{DD} = 10.8 \text{ V}$, $V_{SS} = 0 \text{ V}$ $V_S = 1 \text{ V}/10 \text{ V}$, $V_D = 10 \text{ V}/0 \text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.02 ± 0.55	± 2	± 12.5	nA typ nA max	$V_S = 1 \text{ V}/10 \text{ V}$, $V_D = 10 \text{ V}/0 \text{ V}$; see Figure 24
Channel On Leakage, I_D , I_S (On)	± 0.15 ± 1.5	± 4	± 30	nA typ nA max	$V_S = V_D = 1 \text{ V}/10 \text{ V}$; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	170 250	295	330	ns typ ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 8 \text{ V}$; see Figure 30
t_{OFF}	75 135	165	190	ns typ ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 8 \text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_D (ADG1413 Only)	100		40	ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
Charge Injection, Q_{INJ}	30			ns min	$V_{S1} = V_{S2} = 8 \text{ V}$; see Figure 31
Off Isolation	−80			pC typ	$V_S = 6 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 32
Channel-to-Channel Crosstalk	−100			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 26
−3 dB Bandwidth	130			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 27
Insertion Loss	−0.5			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 28
C_S (Off)	38			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 28
C_D (Off)	40			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D , C_S (On)	104			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001 220		1 380	μA typ μA max μA typ μA max	$V_{DD} = 13.2 \text{ V}$ Digital inputs = 0 V or V_{DD} Digital inputs = 5 V
V_{DD}			5/16.5	V min/V max	$GND = 0 \text{ V}$, $V_{SS} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

±5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance, R _{ON}	3.3	4.9	5.4	Ω typ	V _S = ±4.5 V, I _S = −10 mA; see Figure 23 V _{DD} = +4.5 V, V _{SS} = −4.5 V
	4			Ω max	
On-Resistance Match Between Channels, ΔR _{ON}	0.13			Ω typ	V _S = ±4.5 V, I _S = −10 mA
	0.22	0.23	0.25	Ω max	V _S = ±4.5 V; I _S = −10 mA
On-Resistance Flatness, R _{FLAT(ON)}	0.9			Ω typ	
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.03	±2	±12.5	nA typ	V _{DD} = +5.5 V, V _{SS} = −5.5 V V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 24
	±0.55			nA max	
Drain Off Leakage, I _D (Off)	±0.03			nA typ	V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I _D , I _S (On)	±0.05			nA typ	V _S = V _D = ±4.5 V; see Figure 25
	±1.0	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001		±0.1	μA typ	
				μA max	
Digital Input Capacitance, C _{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t _{ON}	275	465	510	ns typ	R _L = 300 Ω, C _L = 35 pF
	400			ns max	V _S = 3 V; see Figure 30
t _{OFF}	175	320	380	ns typ	R _L = 300 Ω, C _L = 35 pF
	290			ns max	V _S = 3 V; see Figure 30
Break-Before-Make Time Delay, t _D (ADG1413 Only)	100			ns typ	R _L = 300 Ω, C _L = 35 pF
			50	ns min	V _{S1} = V _{S2} = 3 V; see Figure 31
Charge Injection, Q _{INJ}	30			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 32
Off Isolation	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−100			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	R _L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	130			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
Insertion Loss	−0.5			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
C _S (Off)	32			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	33			pF typ	V _S = 0 V, f = 1 MHz
C _D , C _S (On)	116			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1.0	μA typ	V _{DD} = +5.5 V, V _{SS} = −5.5 V Digital inputs = 0 V or V _{DD}
			μA max		
I _{SS}	0.001		1.0	μA typ	Digital inputs = 0 V or V _{DD}
				μA max	
V _{DD} /V _{SS}			±4.5/±16.5	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V _{DD} to V _{SS}	35 V
V _{DD} to GND	−0.3 V to +25 V
V _{SS} to GND	+0.3 V to −25 V
Analog Inputs ¹	V _{SS} − 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs ¹	GND − 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	500 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel at 25°C	
16-Lead TSSOP	190 mA
16-Lead LFCSP	250 mA
Continuous Current per Channel at 125°C	
16-Lead TSSOP	90 mA
16-Lead LFCSP	100 mA
Operating Temperature Range Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ _{JA} Thermal Impedance (Four-Layer Board)	112°C/W
16-Lead LFCSP, θ _{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

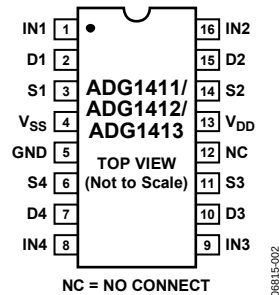
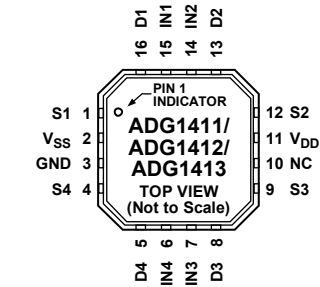


Figure 2. TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .
2. NC = NO CONNECT.

Figure 3. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. This pin can be an input or output.
3	1	S1	Source Terminal. This pin can be an input or output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. This pin can be an input or output.
7	5	D4	Drain Terminal. This pin can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin can be an input or output.
11	9	S3	Source Terminal. This pin can be an input or output.
12	10	NC	No Connection.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin can be an input or output.
15	13	D2	Drain Terminal. This pin can be an input or output.
16	14	IN2	Logic Control Input.

Table 6. ADG1411/ADG1412 Truth Table

ADG1411 INx	ADG1412 INx	Switch Condition
0	1	On
1	0	Off

Table 7. ADG1413 Truth Table

ADG1413 INx	S1, S4	S2, S3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

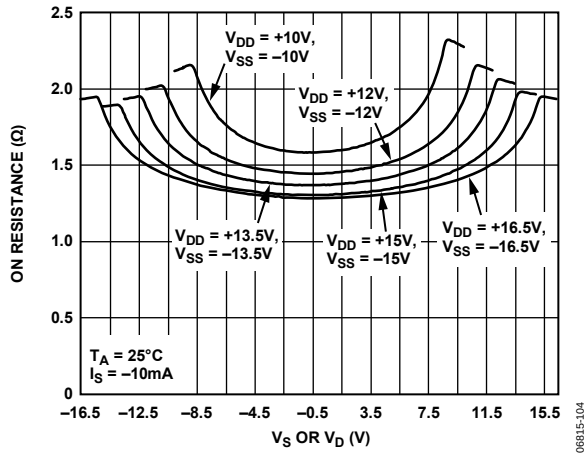


Figure 4. On Resistance vs. V_D or V_S , Dual Supply

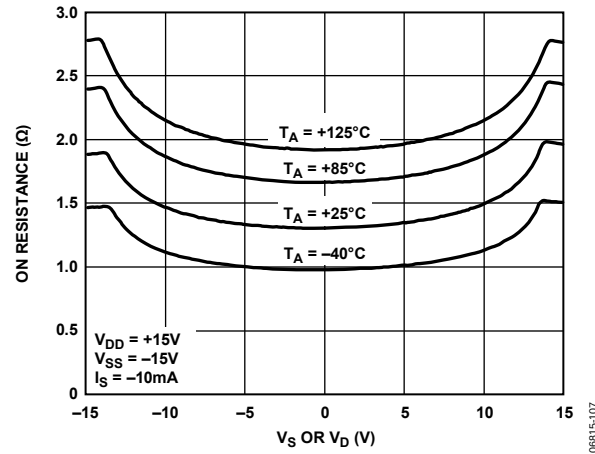


Figure 7. On Resistance vs. V_D or V_S for Different Temperatures, ± 15 V Dual Supply

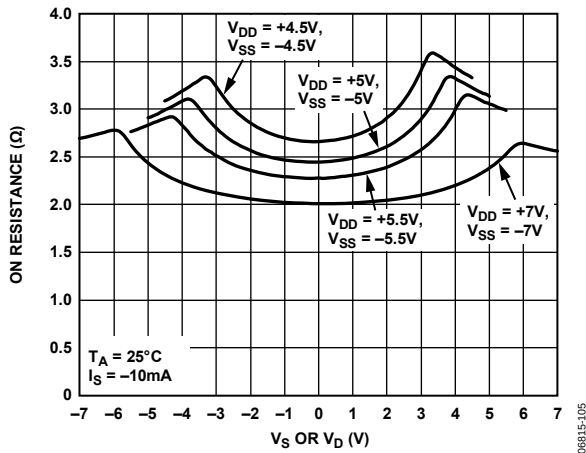


Figure 5. On Resistance vs. V_D or V_S , Dual Supply

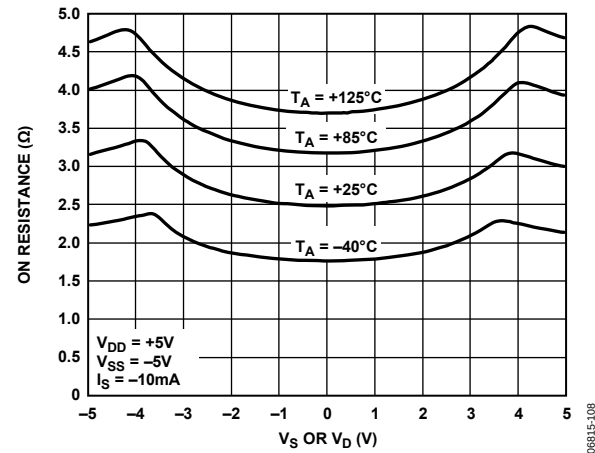


Figure 8. On Resistance vs. V_D or V_S for Different Temperatures, ± 5 V Dual Supply

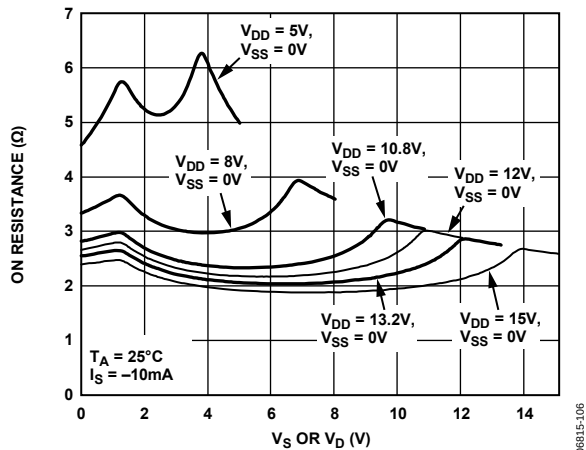


Figure 6. On Resistance vs. V_D or V_S , Single Supply

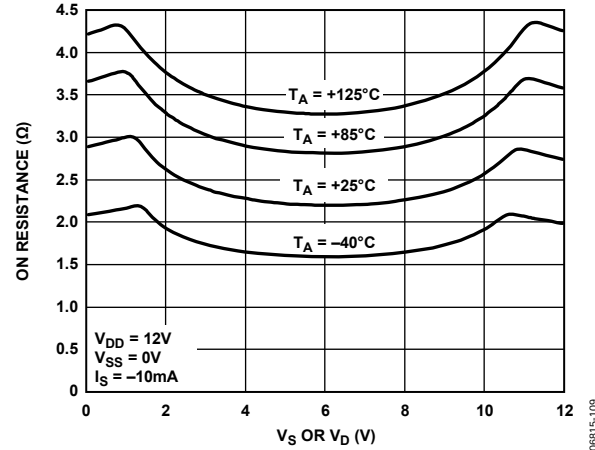


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, +12 V Single Supply

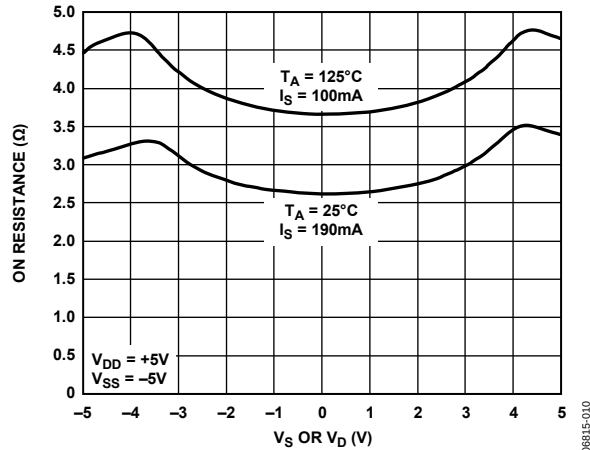


Figure 10. On Resistance vs. V_D or V_S for Different Current Levels, ± 5 V Dual Supply

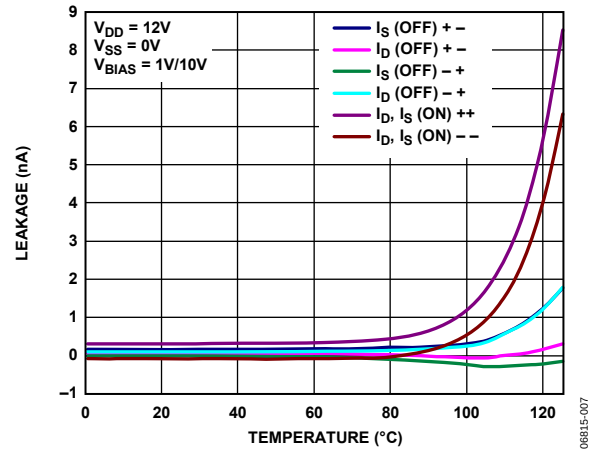


Figure 13. Leakage Currents vs. Temperature, +12 V Single Supply

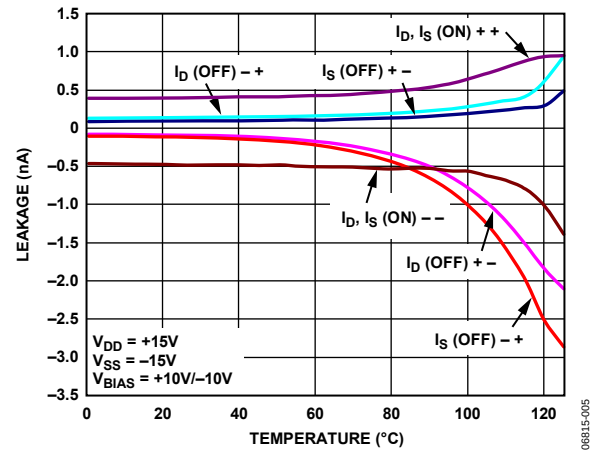


Figure 11. Leakage Currents vs. Temperature, ± 15 V Dual Supply

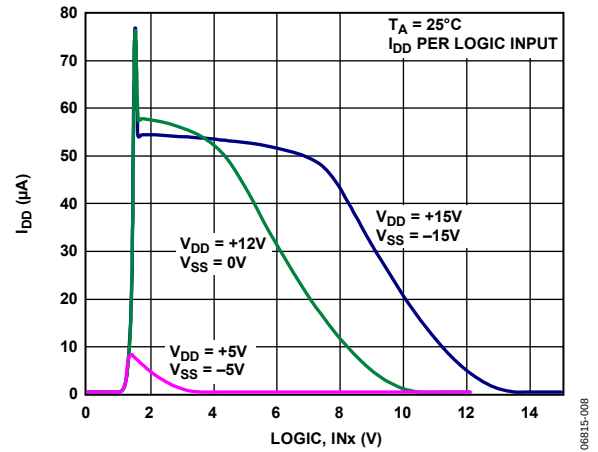


Figure 14. I_{DD} vs. Logic Level

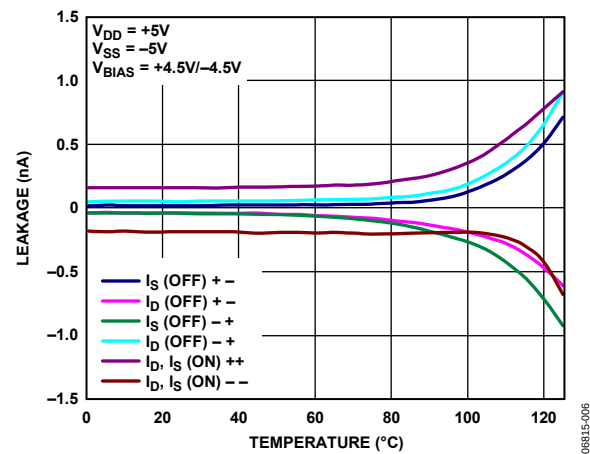


Figure 12. Leakage Currents vs. Temperature, ± 5 V Dual Supply

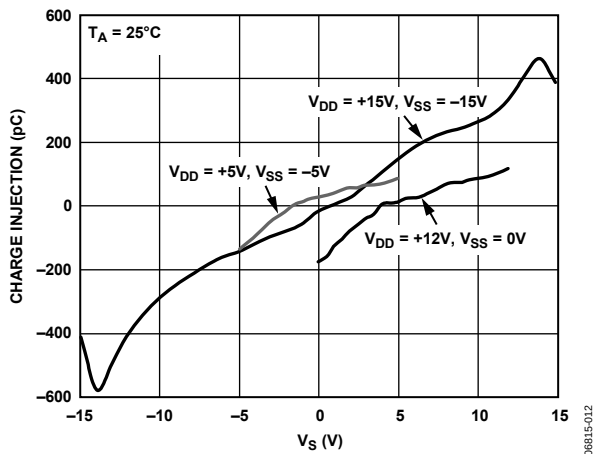


Figure 15. Charge Injection vs. Source Voltage

ADG1411/ADG1412/ADG1413

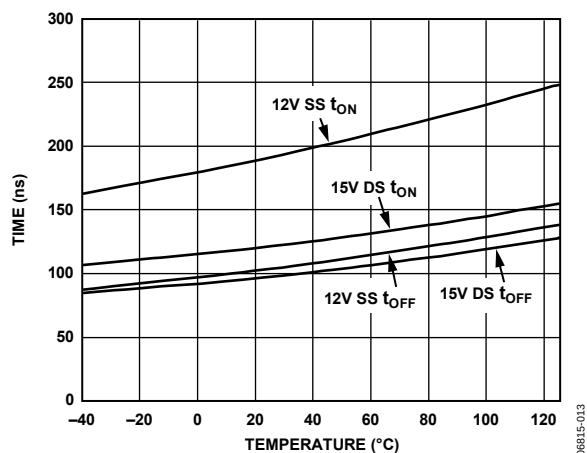


Figure 16. t_{ON}/t_{OFF} Times vs. Temperature for Single Supply (SS) and Dual Supply (DS)

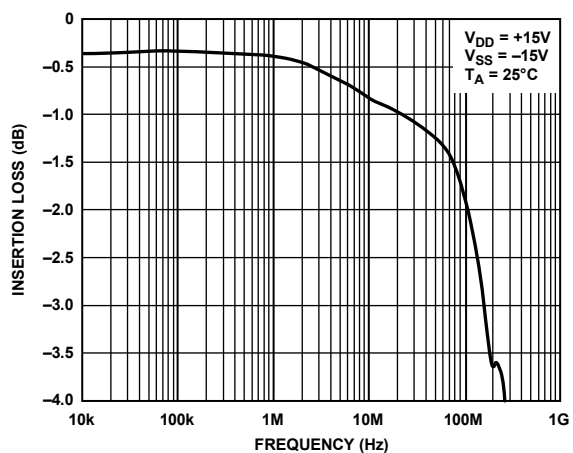


Figure 19. On Response vs. Frequency, $\pm 15 V$ Dual Supply

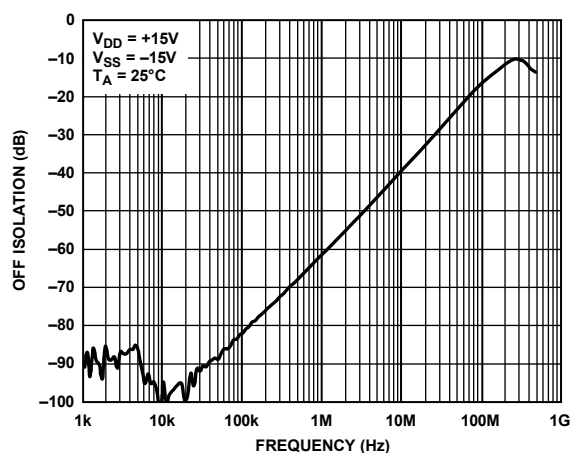


Figure 17. Off Isolation vs. Frequency, $\pm 15 V$ Dual Supply

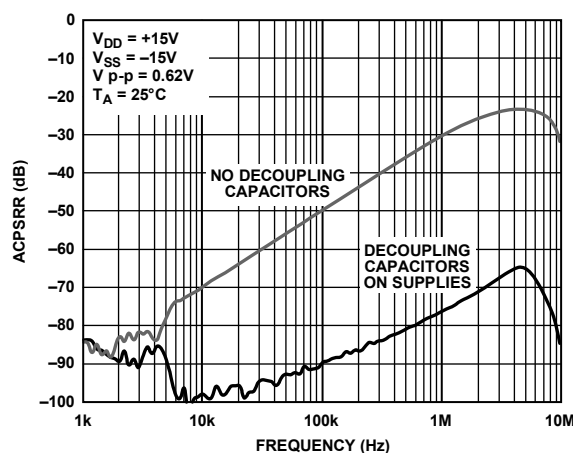


Figure 20. ACPSRR vs. Frequency, $\pm 15 V$ Dual Supply

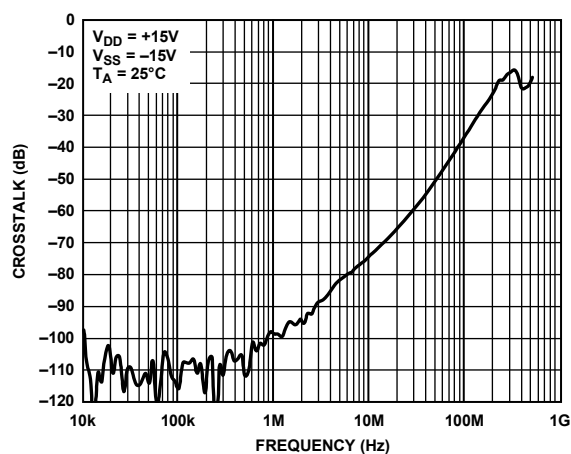


Figure 18. Crosstalk vs. Frequency, $\pm 15 V$ Dual Supply

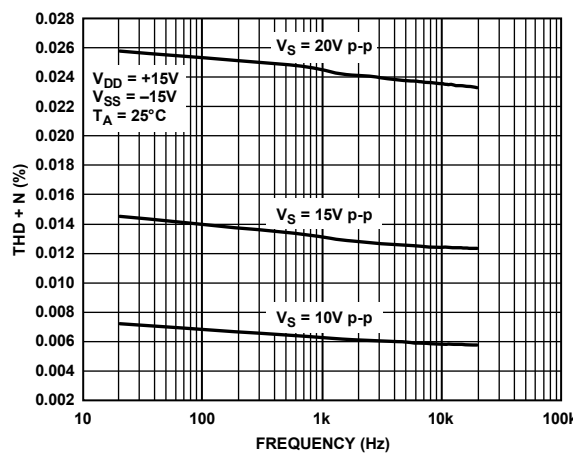


Figure 21. THD + N vs. Frequency, $\pm 15 V$ Dual Supply

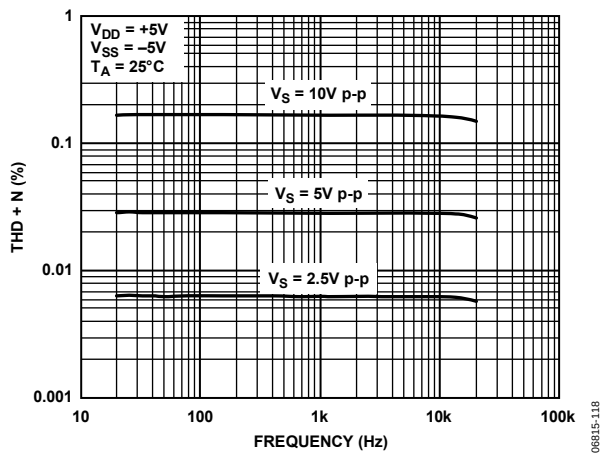


Figure 22. THD + N vs. Frequency, $\pm 5V$ Dual Supply

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D, V_S

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL}, I_{INH}

The input current of the digital input when high or when low.

C_S (Off)

The off switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on. See Figure 30.

t_{OFF}

The delay between applying the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the part's ability to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

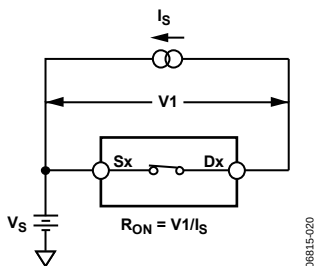


Figure 23. On Resistance

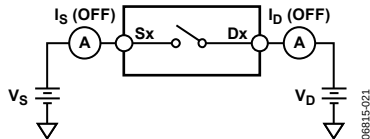


Figure 24. Off Leakage

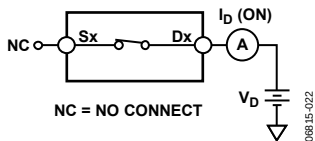


Figure 25. On Leakage

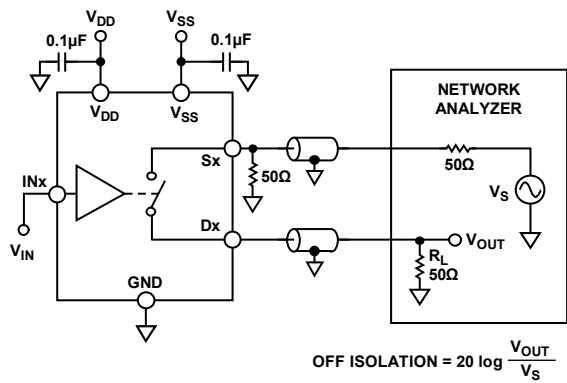


Figure 26. Off Isolation

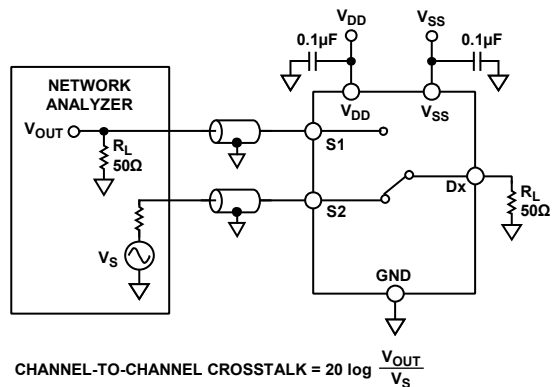


Figure 27. Channel-to-Channel Crosstalk

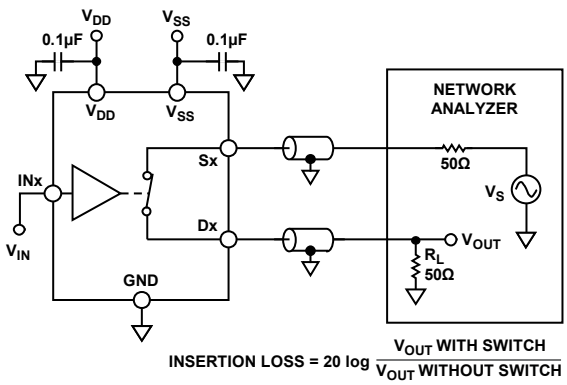


Figure 28. Bandwidth

ADG1411/ADG1412/ADG1413

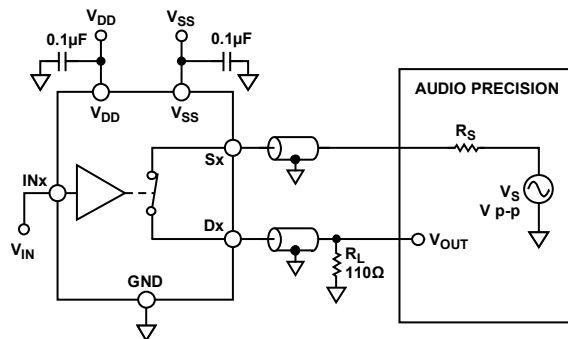


Figure 29. THD + Noise

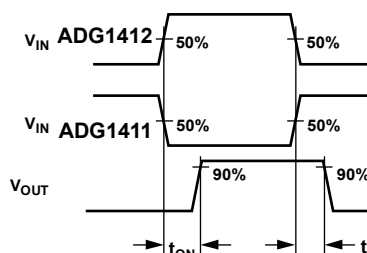
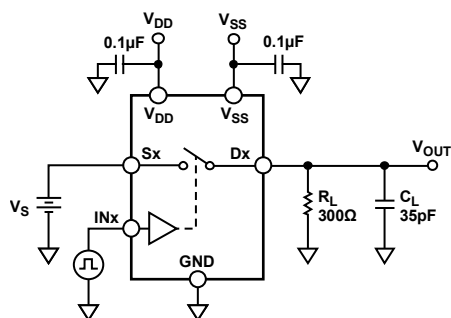


Figure 30. Switching Times

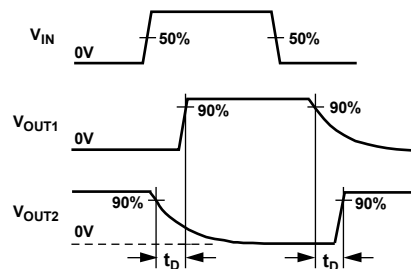
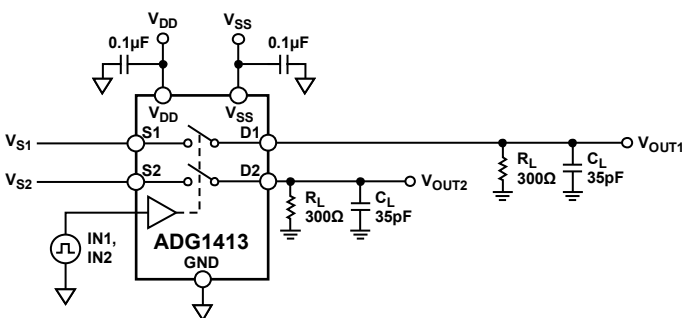


Figure 31. Break-Before-Make Time Delay

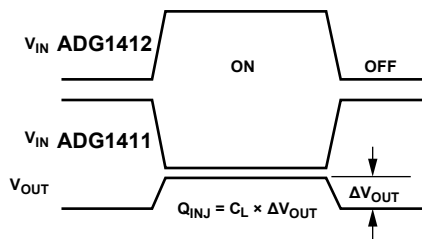
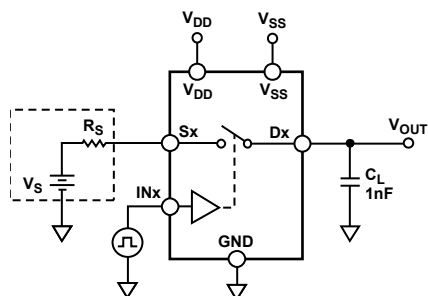
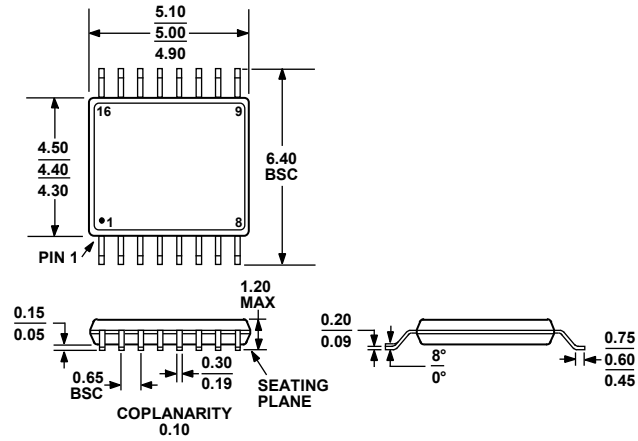


Figure 32. Charge Injection

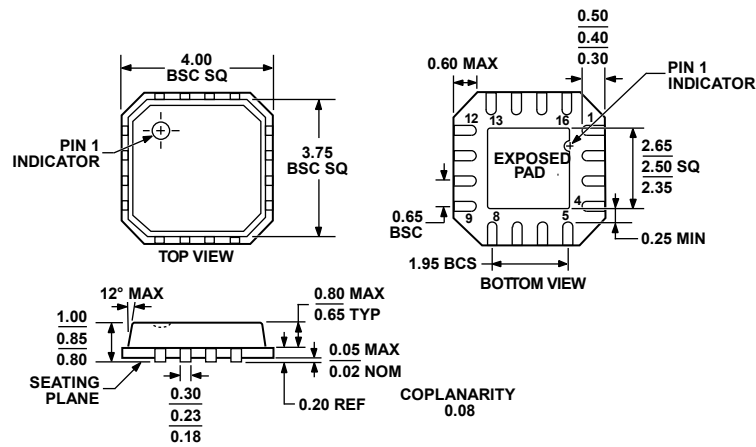
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm x 4 mm Body, Very Thin Quad
(CP-16-13)

Dimensions shown in millimeters

031005-A

ADG1411/ADG1412/ADG1413

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1411YRUZ ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1411YRUZ-REEL7 ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1411YCPZ-REEL ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1411YCPZ-REEL7 ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1412YRUZ ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1412YRUZ-REEL7 ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1412YCPZ-REEL ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1412YCPZ-REEL7 ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1413YRUZ ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1413YRUZ-REEL7 ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1413YCPZ-REEL ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1413YCPZ-REEL7 ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13

¹ Z = RoHS Compliant Part.