

# FDMS86200DC

## N-Channel Dual Cool™ Shielded Gate PowerTrench® MOSFET 150 V, 40 A, 17 mΩ

### Features

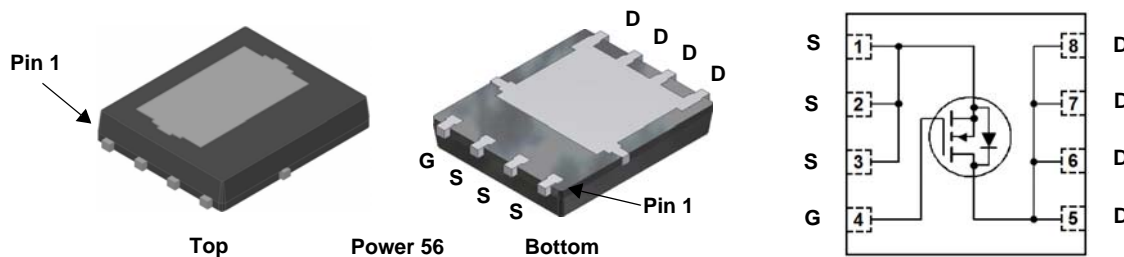
- Shielded Gate MOSFET Technology
- Dual Cool™ Top Side Cooling PQFN package
- Max  $r_{DS(on)}$  = 17 mΩ at  $V_{GS} = 10$  V,  $I_D = 9.3$  A
- Max  $r_{DS(on)}$  = 25 mΩ at  $V_{GS} = 6$  V,  $I_D = 7.8$  A
- High performance technology for extremely low  $r_{DS(on)}$
- 100% UIL tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Applications

- Primary MOSFET in DC - DC converters
- Secondary Synchronous rectifier
- Load switch



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	40	A
	-Continuous $T_A = 25$ °C (Note 1a)	9.3	
	-Pulsed (Note 4)	100	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	294	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	125	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.2	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86200	FDMS86200DC	Dual Cool™ Power 56	13"	12 mm	3000 units

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		105		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	3.3	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-11		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9.3\text{ A}$		14	17	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 7.8\text{ A}$		17	25	
		$V_{GS} = 10\text{ V}$ , $I_D = 9.3\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		29	35	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 9.3\text{ A}$		32		S

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2110	2955	pF
$C_{oss}$	Output Capacitance			205	290	pF
$C_{rss}$	Reverse Transfer Capacitance			8.1	15	pF
$R_g$	Gate Resistance		0.1	1.5	3.0	$\Omega$

#### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 9.3\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		16	29	ns
$t_r$	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
$t_f$	Fall Time			5	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		30	42
	Total Gate Charge	$V_{GS} = 0\text{ V to }6\text{ V}$	$V_{DD} = 75\text{ V}$ $I_D = 9.3\text{ A}$	19	27	nC
$Q_{gs}$	Gate to Source Charge			9.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.6		nC

#### Drain-Source Diode Characteristics

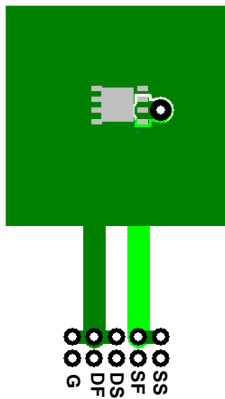
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 9.3\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2.6\text{ A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 9.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		79	126	ns
$Q_{rr}$	Reverse Recovery Charge			126	176	nC

## Thermal Characteristics

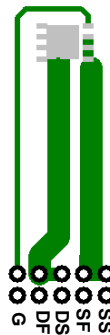
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	13	

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 38  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

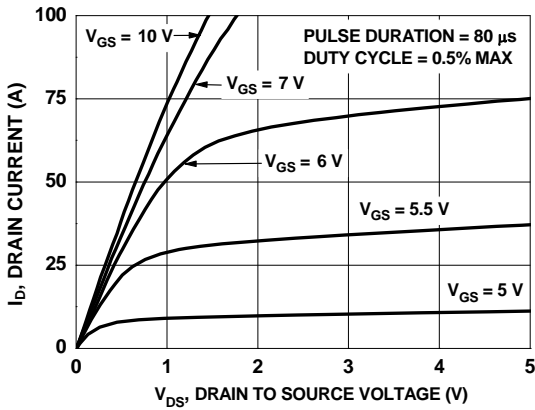
- Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
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- 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

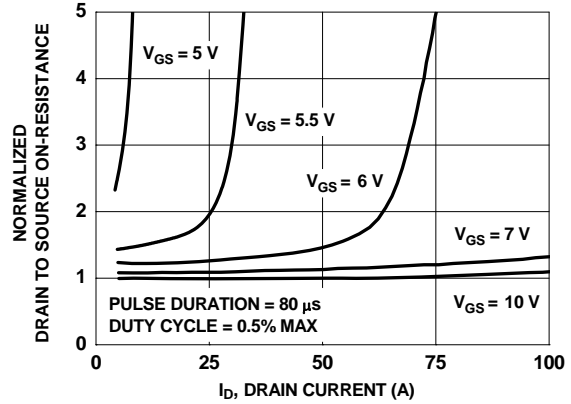
3.  $E_{AS}$  of 294 mJ is based on starting  $T_J = 25^{\circ}\text{C}$ ; N-ch:  $L = 3 \text{ mH}$ ,  $I_{AS} = 14 \text{ A}$ ,  $V_{DD} = 150 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ . 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 42 \text{ A}$ .

4. Pulsed  $I_d$  limited by junction temperature,  $t_d \leq 10 \mu\text{s}$ , please refer to SOA curve for more details.

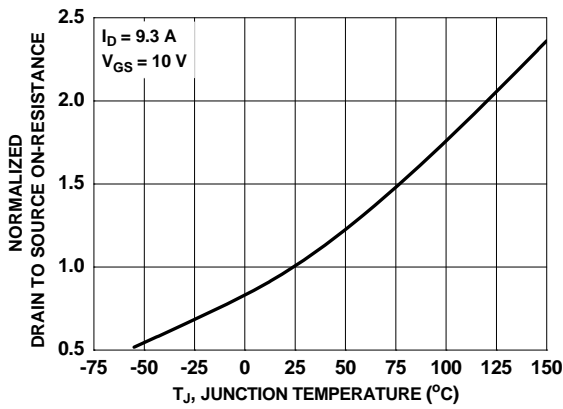
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



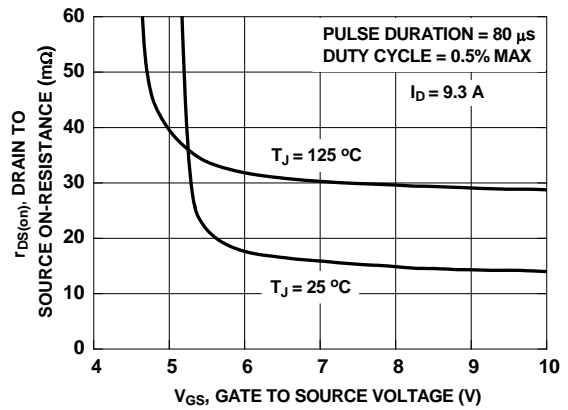
**Figure 1. On-Region Characteristics**



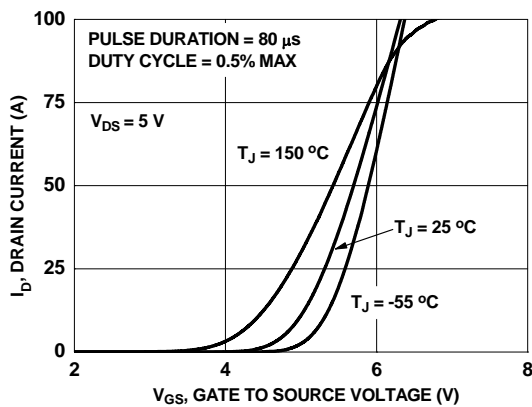
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



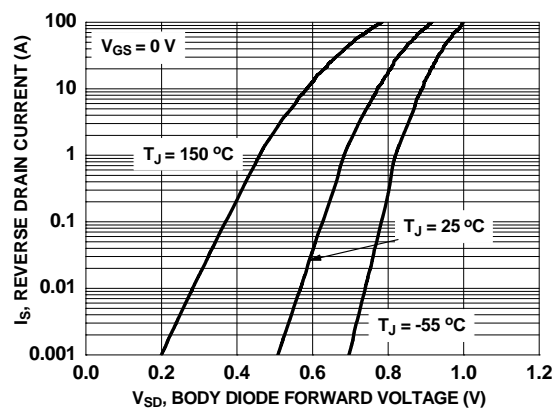
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

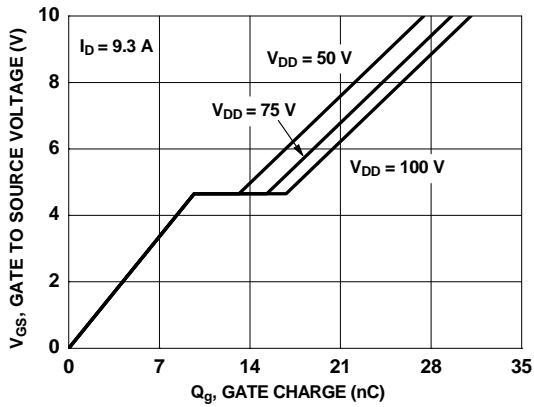


**Figure 5. Transfer Characteristics**

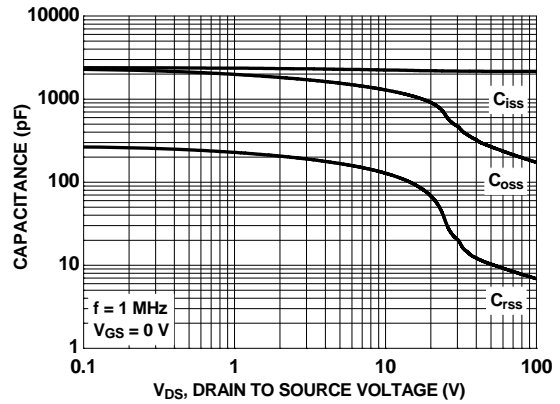


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

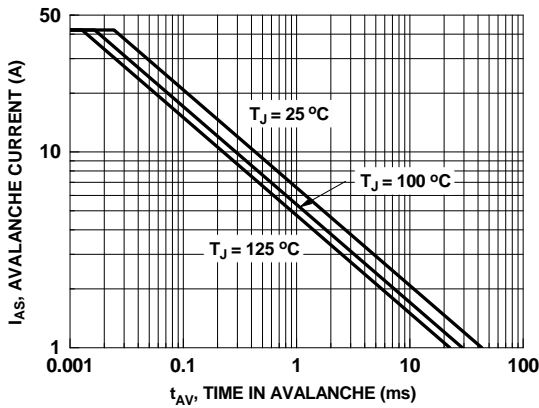
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



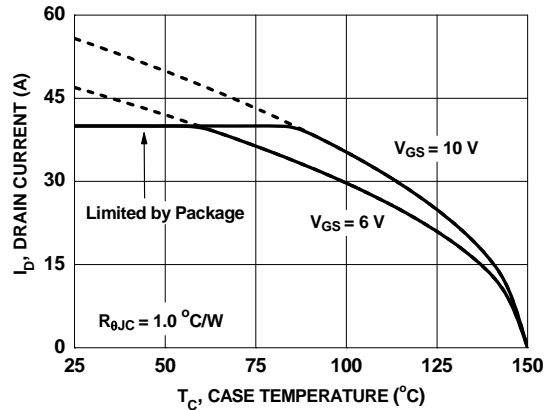
**Figure 7. Gate Charge Characteristics**



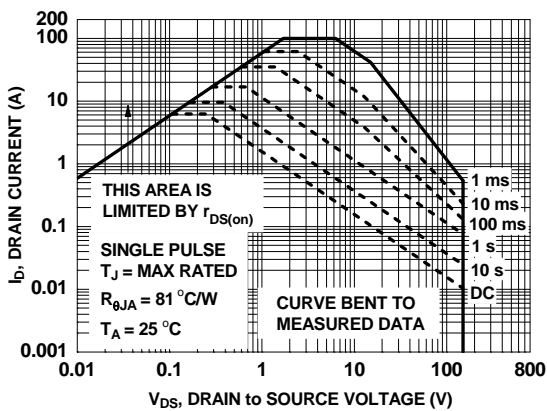
**Figure 8. Capacitance vs Drain to Source Voltage**



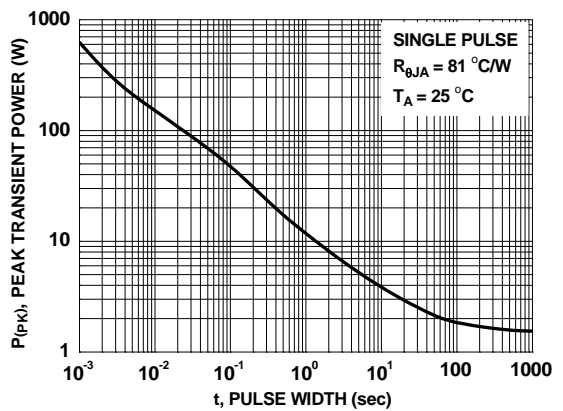
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

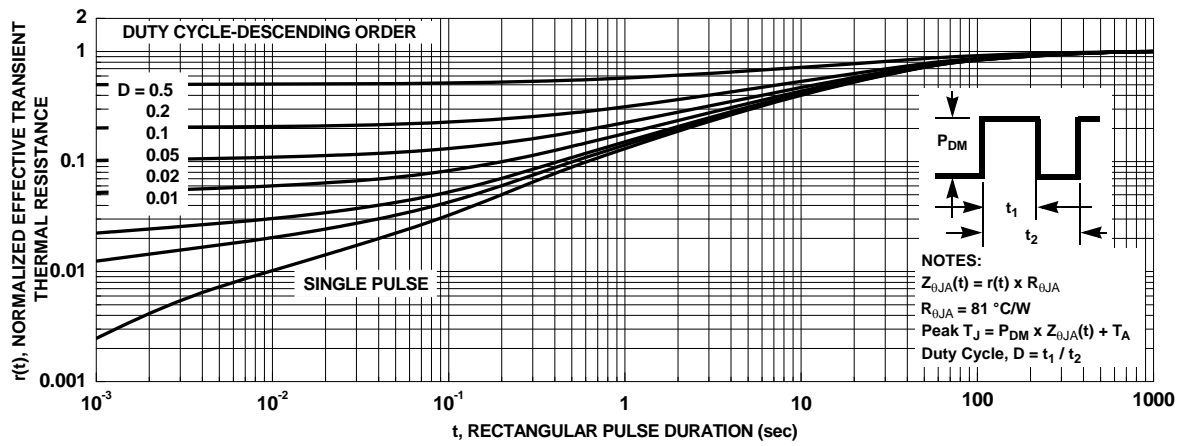


**Figure 11. Forward Bias Safe Operating Area**



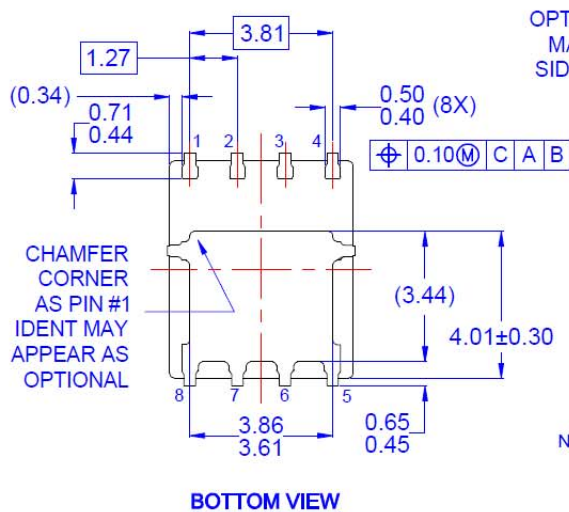
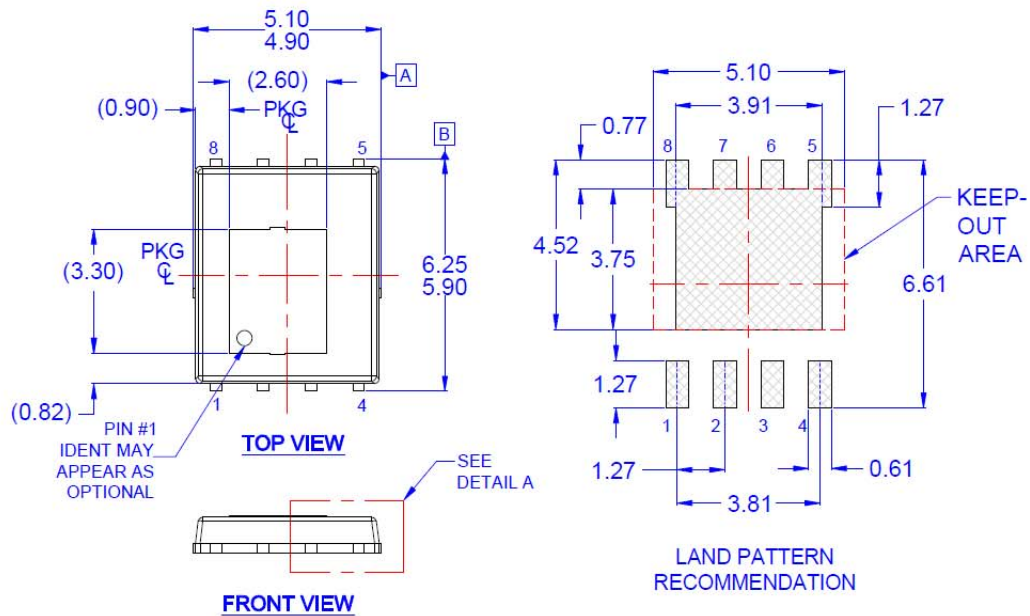
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

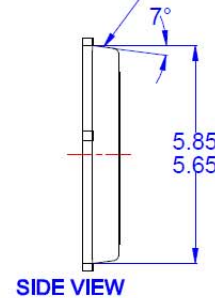


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

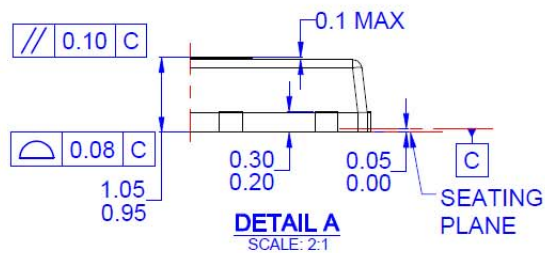
## Dimensional Outline and Pad Layout



OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE








- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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