

Single, dual and quad rail-to-rail input/output 8 MHz operational amplifiers

Datasheet — production data

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 820 μ A typ
- Unity gain stability
- High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- Low input bias current, 1 pA typ
- Low input offset voltage: 1.5 mV max (A grade)
- ESD internal protection $\geq$ 5 kV
- Latch-up immunity

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation
- Automotive applications

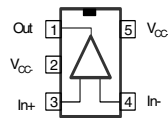
Description

The TSV91x operational amplifiers offer low voltage operation and rail-to-rail input and output, as well as an excellent speed/power consumption ratio, providing an 8 MHz gain-bandwidth product while consuming only 1.1 mA maximum at 5 V. The op-amps are unity gain stable and feature an ultra-low input bias current.

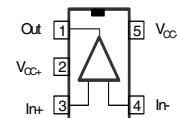
The devices are ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Pin connections (top view)

SOT23-5

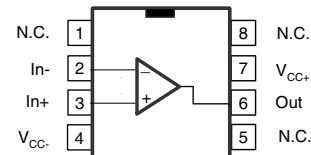


TSV911ILT

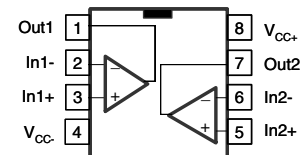


TSV911RILT

SO-8 (single)



MiniSO-8, SO-8, DFN8 2x2 (dual)



SO-14, TSSOP14

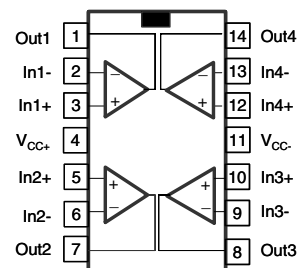


Table 1. Device summary

Reference	Single	Dual	Quad
TSV91x	TSV911	TSV912	TSV914
TSV91xA	TSV911A	TSV912A	TSV914A

1 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	V
V_{in}	Input voltage ⁽³⁾	$V_{CC-} - 0.2$ to $V_{CC+} + 0.2$	V
I_{in}	Input current ⁽⁴⁾	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ^{(5) (6)}		°C/W
	SOT23-5	250	
	DFN8 2x2	57	
	SO-8	125	
	MiniSO-8	190	
	SO-14	103	
R_{thjc}	Thermal resistance junction to case ^{(5) (6)}		°C/W
	SOT23-5	81	
	SO-8	40	
	MiniSO-8	39	
	SO-14	31	
	TSSOP14	32	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁷⁾	5	kV
	MM: machine model ⁽⁸⁾	400	V
	CDM: charged device model ⁽⁹⁾		V
	SOT23-5, SO-8, MiniSO-8	1500	
	TSSOP14	750	
	SO-14	500	
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC} - V_{in}$ must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
8. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
9. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage		
	$-40^{\circ}\text{C} < T_{op} < 125^{\circ}\text{C}$	2.5 to 5.5	V
	$0^{\circ}\text{C} < T_{op} < 125^{\circ}\text{C}$	2.3 to 5.5	
V_{icm}	Common mode input voltage range	$V_{CC-} - 0.1$ to $V_{CC+} + 0.1$	V
T_{oper}	Operating free air temperature range	-40 to +125	$^{\circ}\text{C}$

2 Electrical characteristics

Table 4. Electrical characteristics at $V_{CC+} = +2.5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$		0.1	4.5 7.5	mV
	TSV91xA	$T = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$			1.5 3	
DV_{io}/DT	Input offset voltage drift			5		$\mu\text{V}/^{\circ}\text{C}$
I_{io}	Input offset current ⁽²⁾	$T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
I_{ib}	Input bias current ⁽²⁾	$T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 2.5V , $V_{out} = 1.25\text{V}$, $T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$	58 53	75		dB
A_{vd}	Large signal voltage gain	$R_L = 10\text{k}\Omega$, $V_{out} = 0.5\text{V}$ to 2V , $T = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$	80 75	89		dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10\text{k}\Omega$ $T_{min} < T_{op} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		15 45	40 40 150 150	mV
V_{OL}	Low level output voltage	$R_L = 10\text{k}\Omega$ $T_{min} < T_{op} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		15 45	40 40 150 150	mV
I_{out}	I_{sink}	$V_o = 2.5\text{V}$, $T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	32		mA
	I_{source}	$V_o = 0\text{V}$, $T_{op} = 25^{\circ}\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	35		
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		0.78	1.1 1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $f = 100\text{kHz}$, $T_{op} = 25^{\circ}\text{C}$		8		MHz
F_u	Unity gain frequency	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^{\circ}\text{C}$		7.2		MHz
ϕ_m	Phase margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^{\circ}\text{C}$		45		Degrees
G_m	Gain margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^{\circ}\text{C}$		8		dB
SR	Slew rate	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $A_v = 1$, $T_{op} = 25^{\circ}\text{C}$		4.5		$\text{V}/\mu\text{s}$

Table 4. Electrical characteristics at $V_{CC+} = +2.5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f = 10\text{ kHz}$, $T_{op} = 25^\circ\text{C}$		21		$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G=1$, $f=1\text{ kHz}$, $R_L=2\text{ k}\Omega$, $Bw=22\text{ kHz}$, $T_{op}=25^\circ\text{C}$, $V_{icm}=(V_{CC+1})/2$, $V_{out}=1.1V_{pp}$		0.001		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Guaranteed by design.

Table 5. Electrical characteristics at $V_{CC+} = +3.3\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		0.1	4.5 7.5	mV
	TSV91xA	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$			1.5 3	
DV_{io}	Input offset voltage drift			5		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current ⁽²⁾	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
I_{ib}	Input bias current ⁽²⁾	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 3.3 V , $V_{out} = 1.65\text{ V}$ $T_{min} < T_{op} < T_{max}$	60 55	78		dB
A_{vd}	Large signal voltage gain	$R_L=10\text{ k}\Omega$, $V_{out}=0.5\text{ V}$ to 2.8 V , $T=25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	80 75	90		dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		15	40 40	mV
		$R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		45	150 150	
V_{OL}	Low level output voltage	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		15	40 40	mV
		$R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		45	150 150	
I_{out}	I_{sink}	$V_o = 3.3\text{ V}$, $T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	32		mA
	I_{source}	$V_o = 0\text{ V}$, $T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	35		
I_{CC}	Supply current (per operator)	No load, $V_{out}=V_{CC}/2$ $T_{min} < T_{op} < T_{max}$		0.8	1.1 1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L=2\text{ k}\Omega$, $C_L=100\text{ pF}$, $f=100\text{ kHz}$, $T_{op}=25^\circ\text{C}$		8		MHz

Table 5. Electrical characteristics at $V_{CC+} = +3.3\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_u	Unity gain frequency	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		7.2		MHz
ϕ_m	Phase margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		45		Degrees
G_m	Gain margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		8		dB
SR	Slew rate	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $A_v = 1$, $T_{op} = 25^\circ\text{C}$		4.5		V/ μs
e_n	Equivalent input noise voltage	$f = 10\text{kHz}$, $T_{op} = 25^\circ\text{C}$		21		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
THD+ e_n	Total harmonic distortion	$G = 1$, $f = 1\text{kHz}$, $R_L = 2\text{k}\Omega$, $\text{BW} = 22\text{kHz}$, $V_{icm} = (V_{CC+} + 1)/2$, $V_{out} = 1.9V_{pp}$, $T_{op} = 25^\circ\text{C}$		0.0007		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Guaranteed by design.

Table 6. Electrical characteristics at $V_{CC+} = +5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		0.1	4.5 7.5	mV
	TSV91xA	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$			1.5 3	
DV_{io}	Input offset voltage drift			5	-	$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current ⁽²⁾	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
I_{ib}	Input bias current ⁽²⁾	$T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$		1	10 100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 5V, $V_{out} = 2.5\text{V}$ $T_{min} < T_{op} < T_{max}$	62 58	82	-	dB
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 2.5$ to 5V	70	86	-	dB
A_{vd}	Large signal voltage gain	$R_L = 10\text{k}\Omega$, $V_{out} = 0.5\text{V}$ to 4.5V , $T = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	80 75	91	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10\text{k}\Omega$ $T_{min} < T_{op} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		15 45	40 40 150 150	mV
V_{OL}	Low level output voltage	$R_L = 10\text{k}\Omega$ $T_{min} < T_{op} < T_{max}$ $R_L = 600\Omega$ $T_{min} < T_{op} < T_{max}$		15 45	40 40 150 150	mV

Table 6. Electrical characteristics at $V_{CC+} = +5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out}	I_{sink}	$V_o = 5\text{V}$, $T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	32		mA
	I_{source}	$V_o = 0\text{V}$, $T_{op} = 25^\circ\text{C}$ $T_{min} < T_{op} < T_{max}$	18 16	35		
I_{CC}	Supply current (per operator)	No load, $V_{out} = 2.5\text{V}$ $T_{min} < T_{op} < T_{max}$		0.82	1.1 1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $f = 100\text{kHz}$, $T_{op} = 25^\circ\text{C}$		8		MHz
F_u	Unity gain frequency	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		7.5		MHz
ϕ_m	Phase margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		45		Degrees
G_m	Gain margin	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $T_{op} = 25^\circ\text{C}$		8		dB
SR	Slew rate	$R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $A_V = 1$, $T_{op} = 25^\circ\text{C}$		4.5		V/ μs
e_n	Equivalent input noise voltage	$f = 1\text{kHz}$, $T = 25^\circ\text{C}$ $f = 10\text{kHz}$, $T_{op} = 25^\circ\text{C}$		27 21		$\frac{nV}{\sqrt{\text{Hz}}}$
THD+ e_n	Total harmonic distortion	$G = 1$, $f = 1\text{kHz}$, $R_L = 2\text{k}\Omega$, $Bw = 22\text{kHz}$, $T_{op} = 25^\circ\text{C}$, $V_{icm} = (V_{CC+} + 1)/2$, $V_{out} = 3.6V_{pp}$		0.0004		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Guaranteed by design.

Figure 1. Input offset voltage distribution at $T = 25^{\circ}\text{C}$

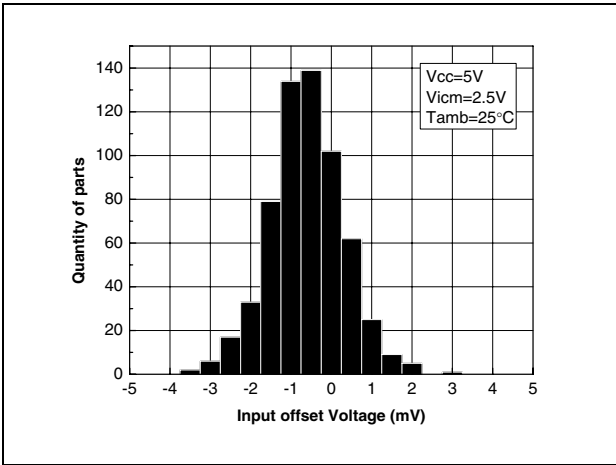


Figure 2. Input offset voltage distribution at $T = 125^{\circ}\text{C}$

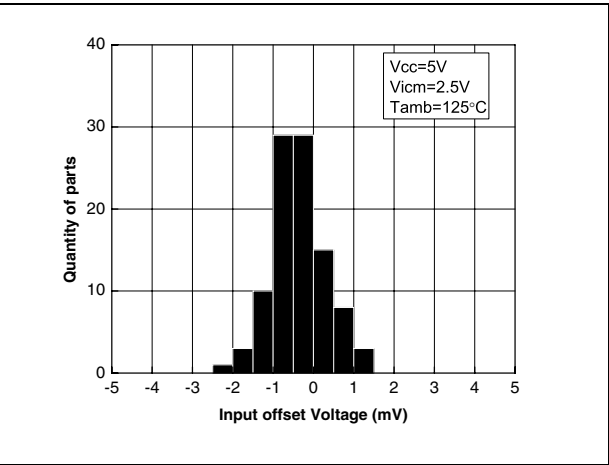


Figure 3. Supply current vs. input common mode voltage at $V_{CC} = 2.5\text{V}$

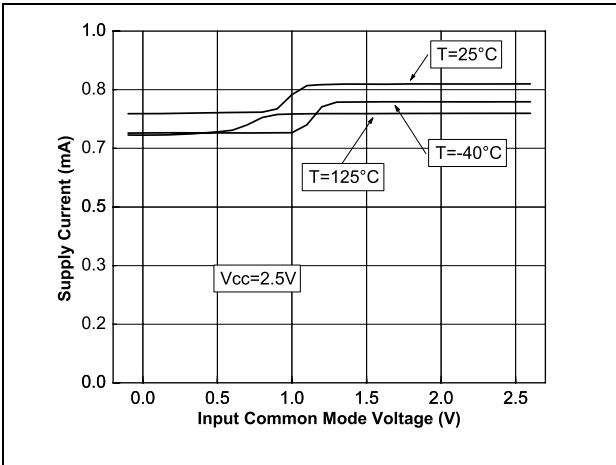


Figure 4. Supply current vs. input common mode voltage at $V_{CC} = 5\text{V}$

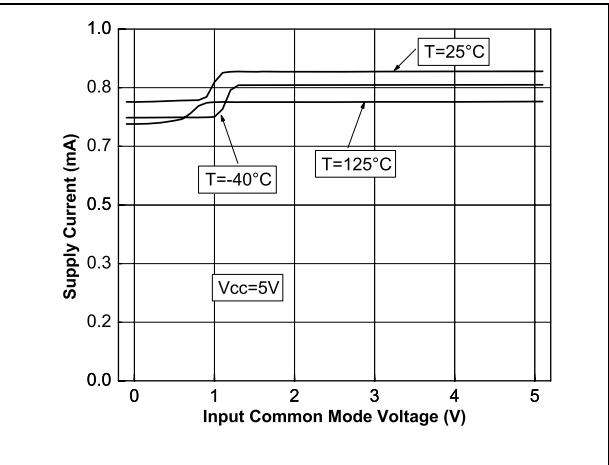


Figure 5. Output current vs. output voltage at $V_{CC} = 2.5\text{V}$

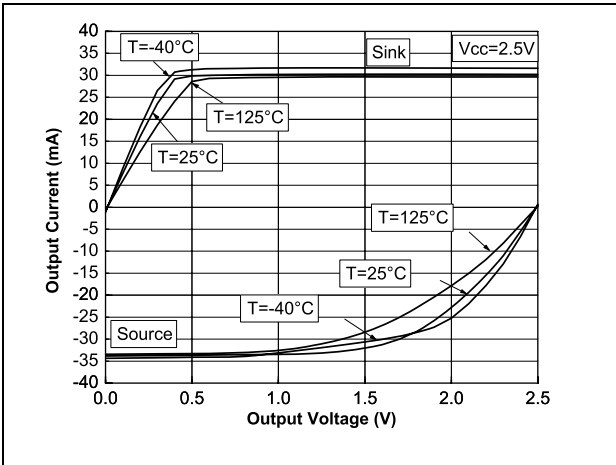


Figure 6. Output current vs. output voltage at $V_{CC} = 5\text{V}$

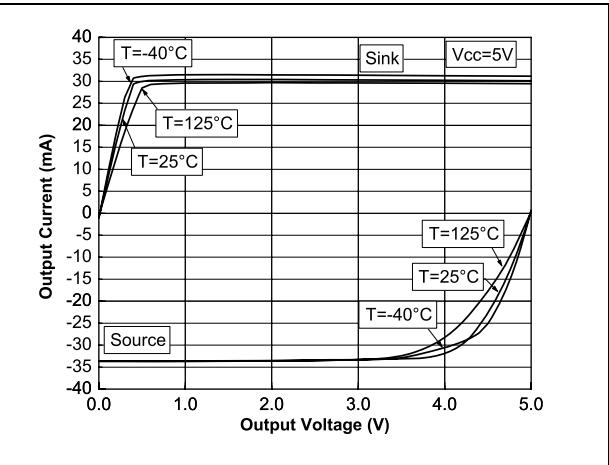


Figure 7. Voltage gain and phase vs. frequency at $V_{CC} = 2.5\text{ V}$ and $V_{icm} = 0.5\text{ V}$

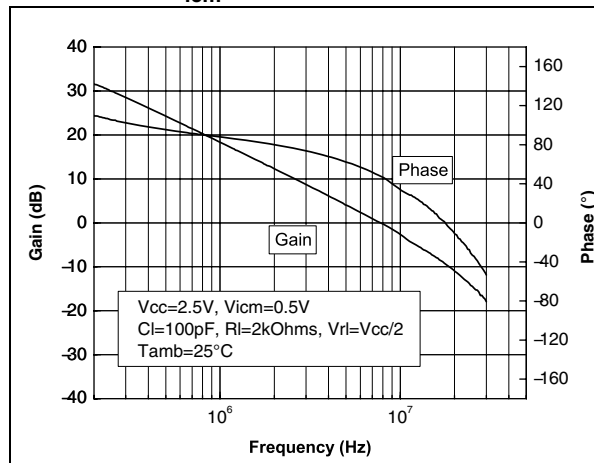


Figure 8. Voltage gain and phase vs. frequency at $V_{CC} = 5.5\text{ V}$ and $V_{icm} = 0.5\text{ V}$

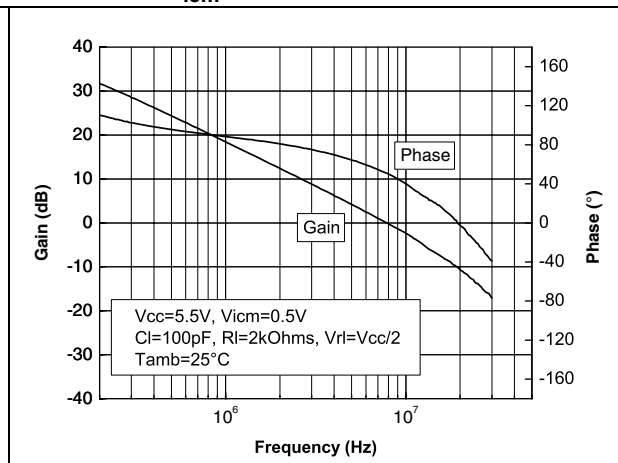


Figure 9. Phase margin vs. capacitive load

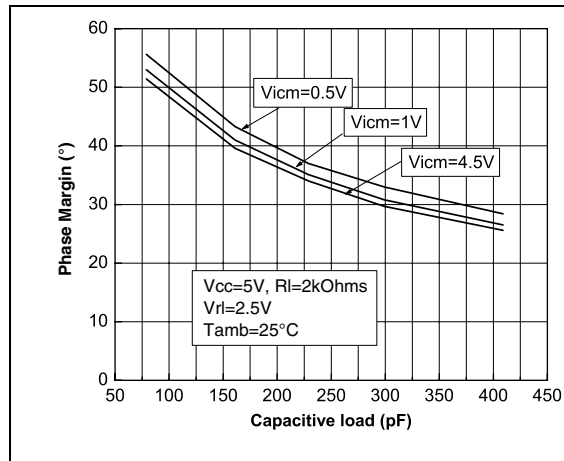


Figure 10. Phase margin vs. output current

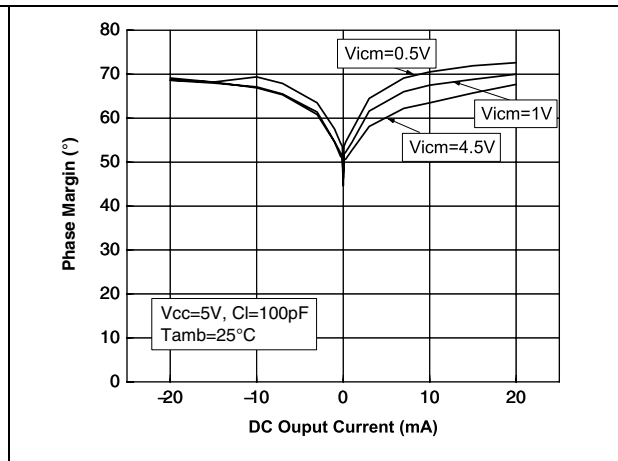


Figure 11. Positive slew rate

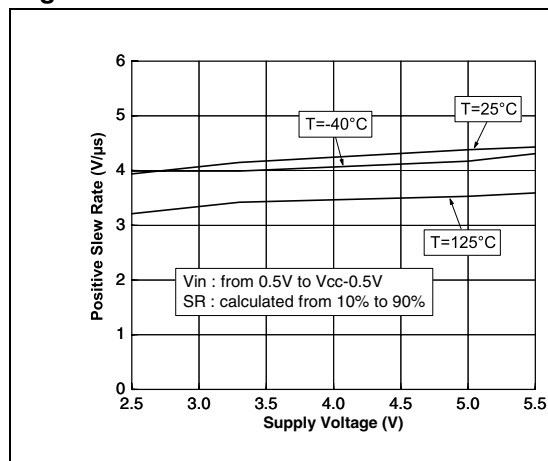


Figure 12. Negative slew rate

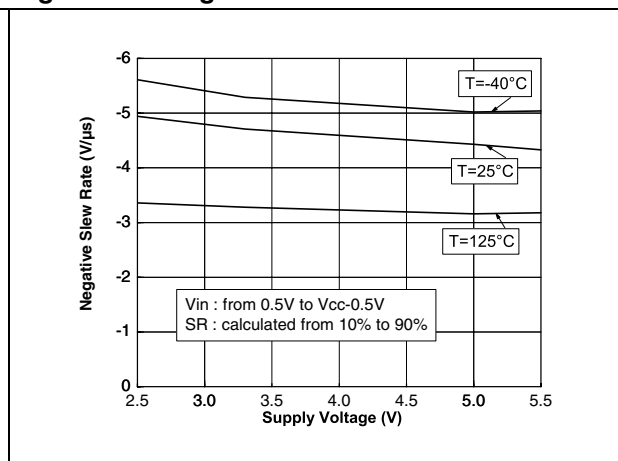


Figure 13. Distortion + noise vs. frequency

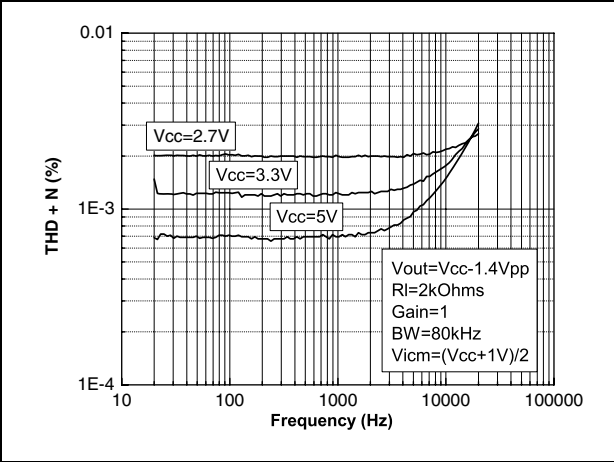


Figure 14. Distortion + noise vs. output voltage

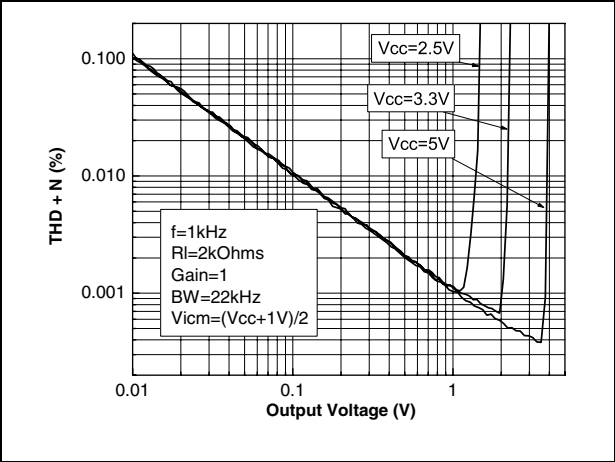


Figure 15. Noise vs. frequency

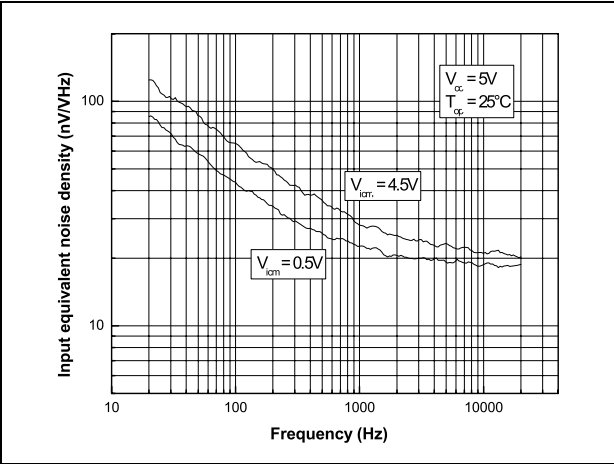


Figure 16. Phase margin vs. capacitive load and serial resistor

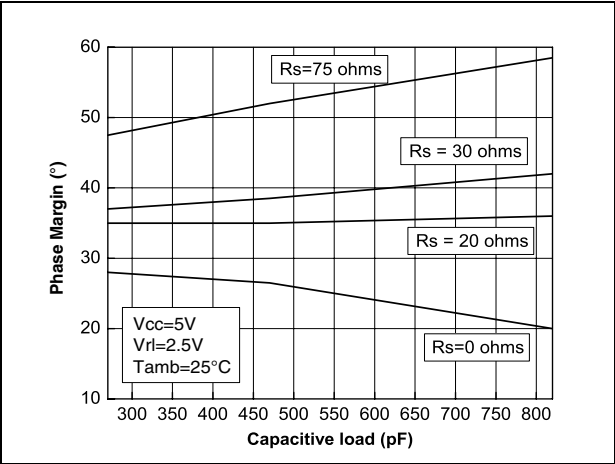
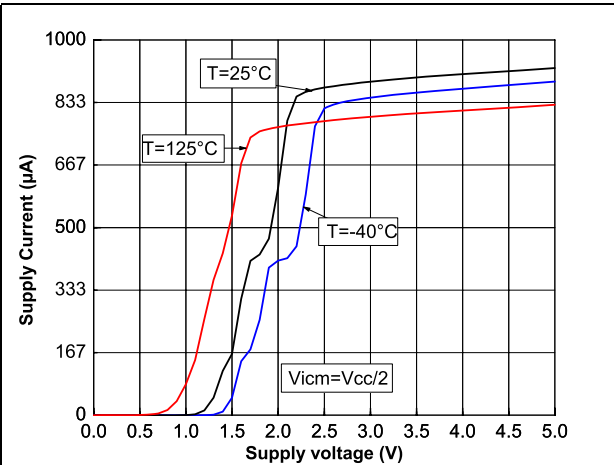


Figure 17. Supply current vs. supply voltage



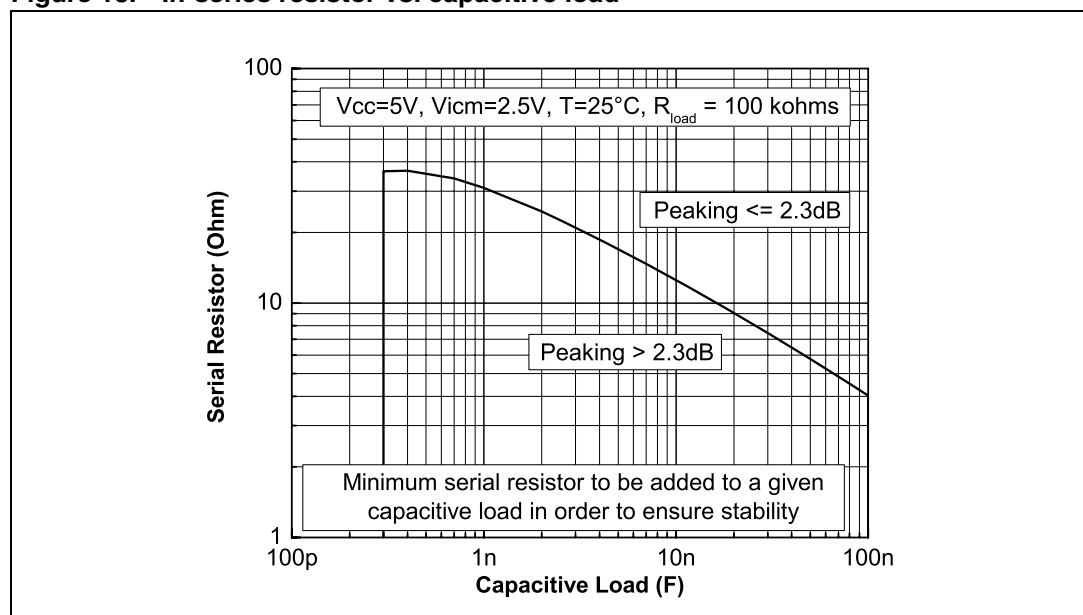
3 Application information

3.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 k Ω

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the device (*Figure 18* shows the recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 18. In-series resistor vs. capacitive load



3.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

3.3 Macromodel

An accurate macromodel of the TSV91x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV91x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 SOT23-5 package information

Figure 19. SOT23-5 package mechanical drawing

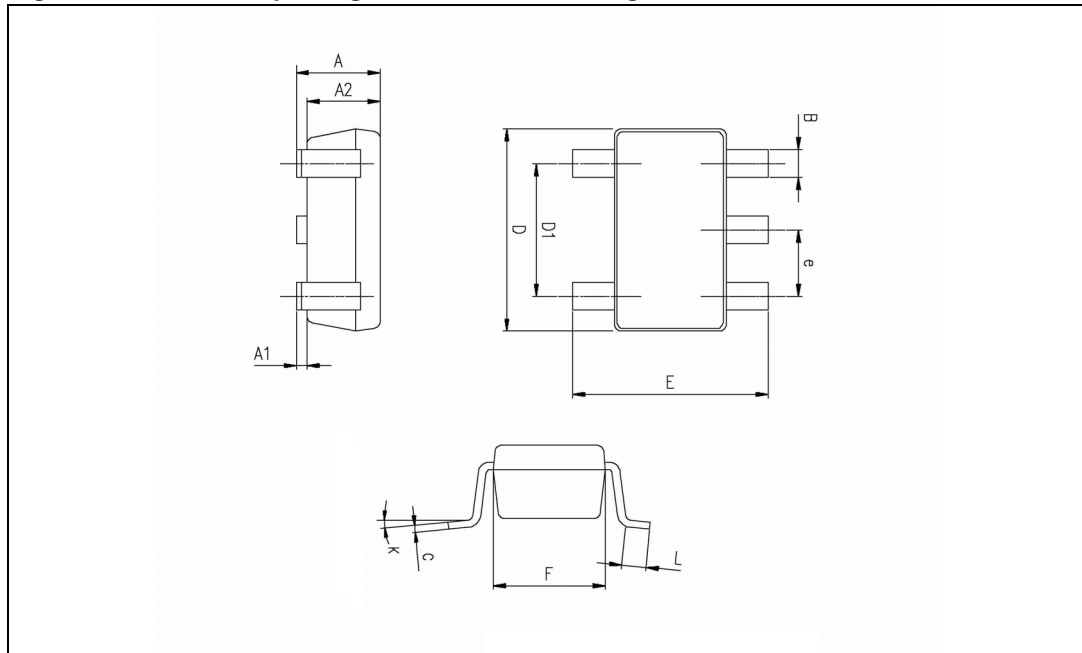


Table 7. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

4.2 DFN8 2x2 mm package information

Figure 20. DFN8 2x2 mm package mechanical drawing

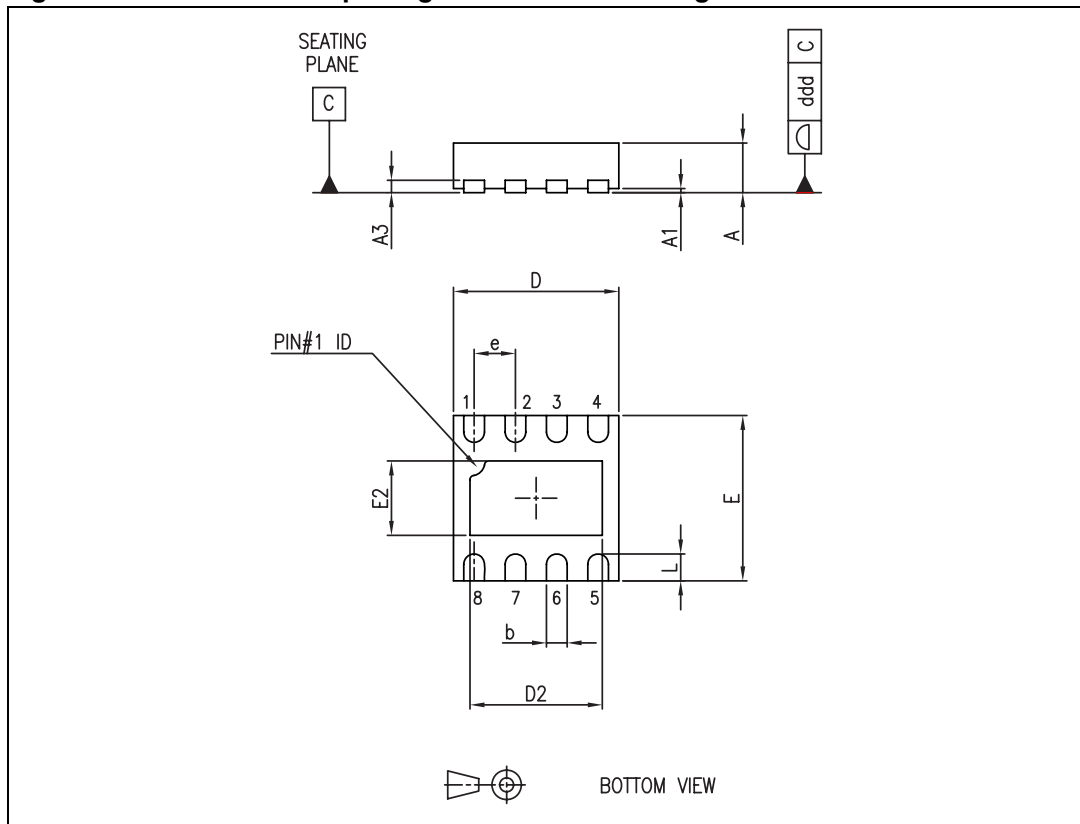
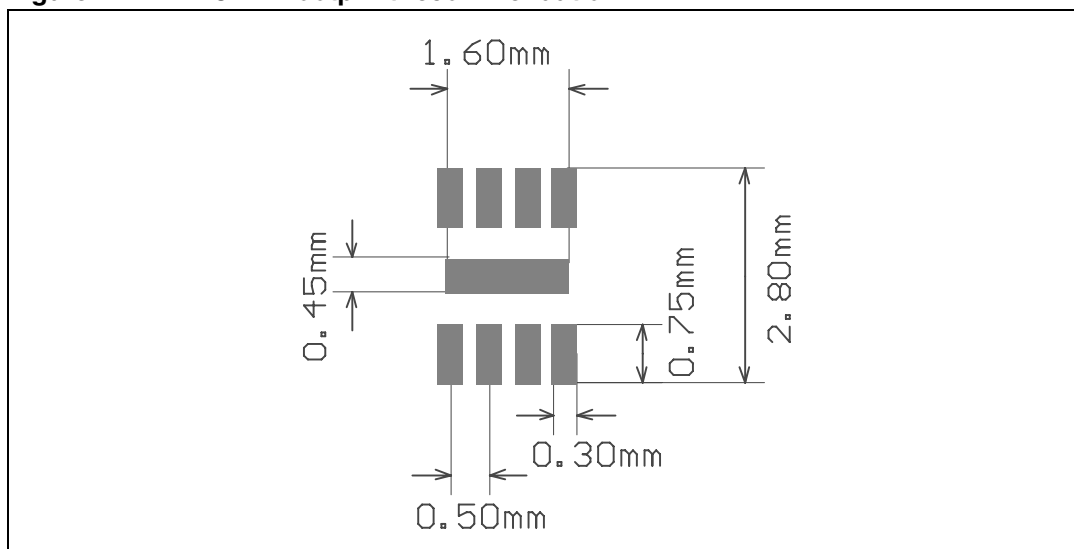


Table 8. DFN8 2x2x0.6 mm package mechanical data (pitch 0.5 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003

Figure 21. DFN8 2x2 footprint recommendation

4.3 MiniSO-8 package information

Figure 22. MiniSO-8 package mechanical drawing

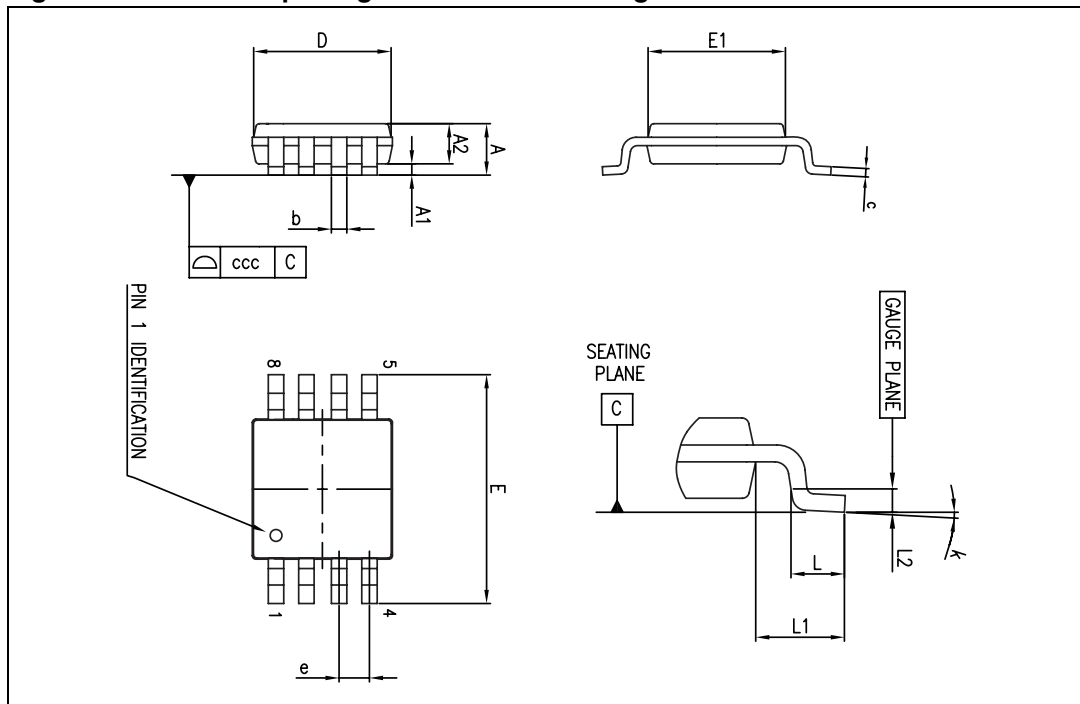


Table 9. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

4.4 SO-8 package information

Figure 23. SO-8 package mechanical drawing

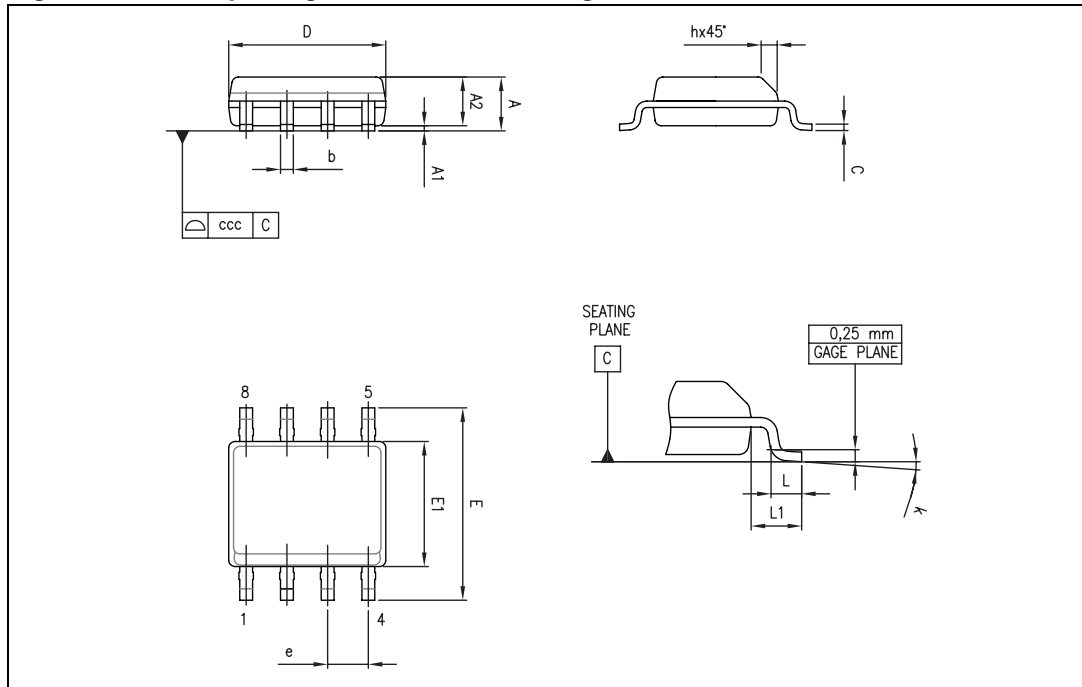


Table 10. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

4.5 TSSOP14 package information

Figure 24. TSSOP14 package mechanical drawing

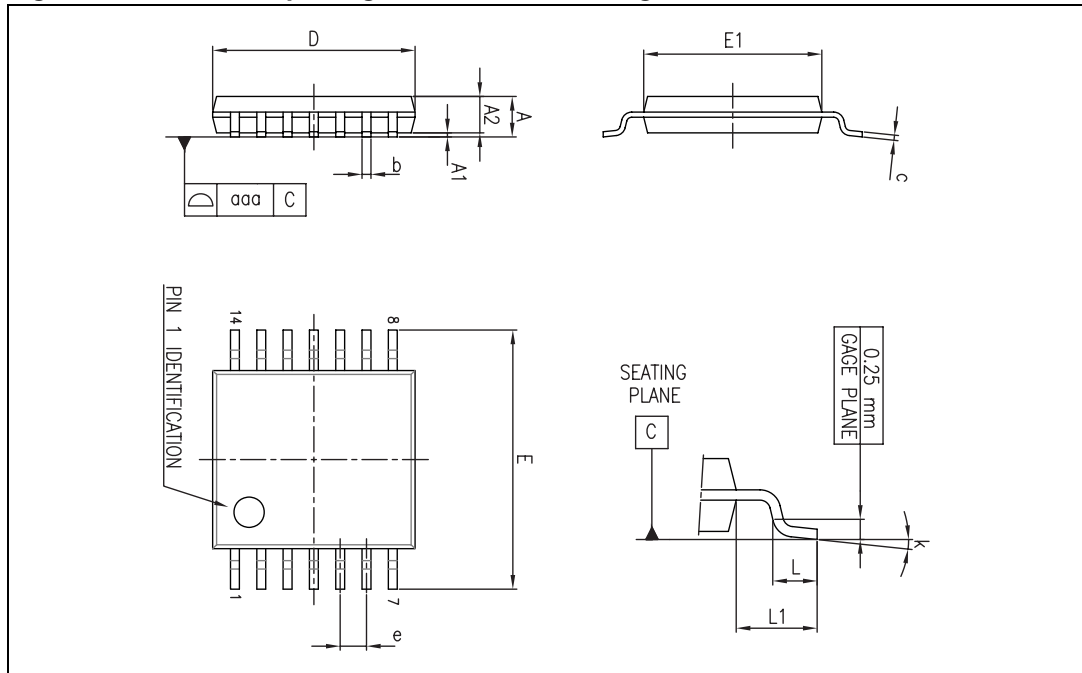


Table 11. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

4.6 SO-14 package information

Figure 25. SO-14 package mechanical drawing

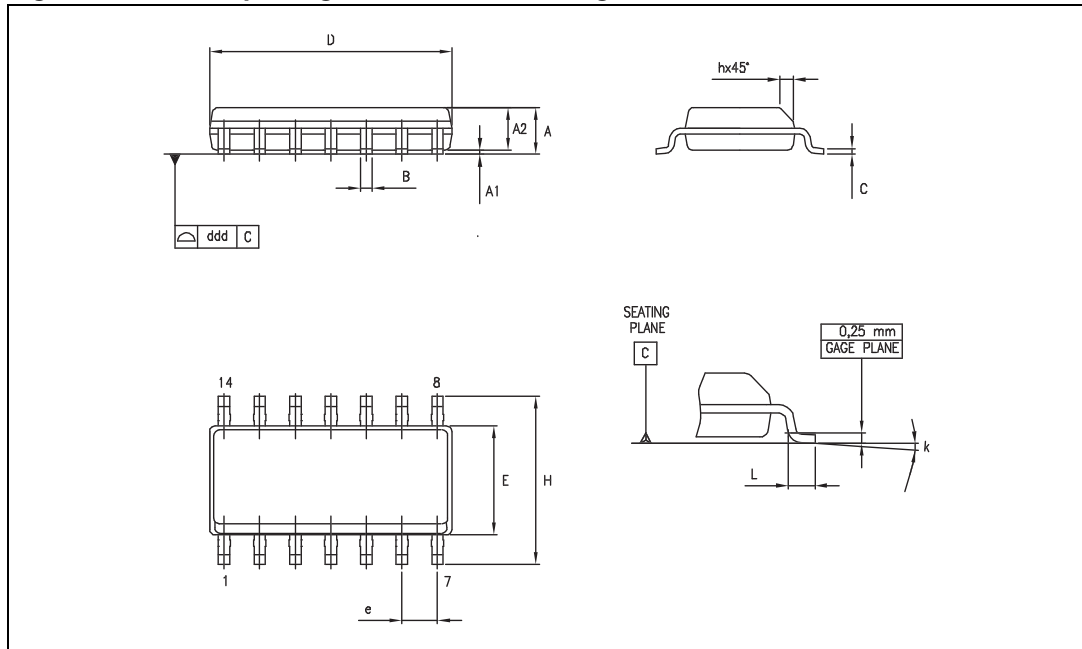


Table 12. SO-14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

5 Ordering information

Table 13. Order codes⁽¹⁾

Order code	Temperature range	Package	Packing	Marking
TSV911ID TSV911IDT	-40°C to +125°C	SO-8	Tube or Tape & reel	V911I
TSV911AID TSV911AIDT				V911AI
TSV911ILT		SOT23-5	Tape & reel	K127
TSV911AILT				K128
TSV911RILT				K125
TSV912IST		MiniSO-8	Tape & reel	K125
TSV912AIST				K126
TSV912ID TSV912IDT		SO-8	Tube or Tape & reel	V912I
TSV912AID TSV912AIDT				V912AI
TSV912IQ2T		DFN8 2x2	Tape & reel	K1Q
TSV914IPT		TSSOP14	Tape & reel	V914I
TSV914IPT				V914AI
TSV914ID TSV914IDT		SO-14 ⁽¹⁾	Tube or Tape & reel	V914I
TSV914AID TSV914AIDT				V914AI
TSV911IYLT ⁽²⁾		SOT23-5 Automotive grade	Tape & reel	K147
TSV911AIYLT ⁽²⁾				K148
TSV911IYDT ⁽²⁾		SO-8 Automotive grade	Tape & reel	V911IY
TSV911AIYDT ⁽²⁾				V911AIY
TSV912IYDT ⁽²⁾				V912IY
TSV912AIYDT ⁽²⁾				V912AY
TSV912IYST ⁽²⁾		MiniSO-8 Automotive grade	Tape & reel	K147
TSV912AIYST ⁽²⁾				K148
TSV914IYDT ⁽²⁾		SO-14 ⁽¹⁾ Automotive grade	Tape & reel	V914IY
TSV914AIYDT ⁽²⁾				V914AY
TSV914IYPT ⁽²⁾		TSSOP14 Automotive grade	Tape & reel	V914IY
TSV914AIYPT ⁽²⁾				V914AY

1. All packages are Moisture Sensitivity Level 1 as per Jedec J-STD-020-C, except SO-14 which is Jedec level 3.

2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
28-Aug-2006	1	First release.
07-Jun-2007	2	Modified ESD CDM parameter for SO-14 package in Table 2: Absolute maximum ratings . Noise parameters updated in Section 2: Electrical characteristics . Added limits in temperature in Section 2: Electrical characteristics . Added automotive grade level description in Table 13: Order codes . Added footnote about SO-14 package in Table 13: Order codes . Added Figure 16: Phase margin vs. capacitive load and serial resistor .
11-Feb-2008	3	Updated footnotes for ESD parameters in Table 2: Absolute maximum ratings . Corrected MiniSO-8 package information in Table 9: MiniSO-8 package mechanical data . Added missing markings for order codes TSV911AILT and TSV912AILT in Table 13: Order codes .
22-Jun-2009	4	Added input current information in Table 2: Absolute maximum ratings . Changed Figure 7 and Figure 8 . Added Chapter 3: Application information . Updated package information in Chapter 4 . Added automotive order codes: TSV911IYLT, TSV911AIYLT, TSV912IYST, TSV912AIYST, TSV914IYPT and TSV914AIYPT in Table 13: Order codes .
17-Sep-2009	5	Added A versions of devices in title on cover page. Modified ESD value for machine model in Table 2: Absolute maximum ratings . Added Figure 17: Supply current vs. supply voltage on page 10 .
18-Mar-2010	6	Added TSV911RILT in Table 13: Order codes , housed in a SOT23-5 package with a new pinout.
24-Jun-2010	7	Added pin connections for TSV911ILT and TSV91RILT on cover page. Added Table 1: Device summary on cover page. Modified supply voltage value in Table 3 . Corrected typical value of DV_{IO} in Table 4 , Table 5 and Table 6 . Added TSV911RILT, TSV911IYDT and TSV911AIYDT order codes in Table 13 . Modified Note 2 under Table 13 .
06-Mar-2012	8	Added DFN8 2x2 package and ordering information for TSV912 device to Chapter 4 and Chapter 5 .

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