OPA4188 0.03-μV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers

1 Features

- Low Offset Voltage: 25 μV (Maximum)
- Zero-Drift: 0.03 μV/°C
- Low Noise: 8.8 nV/√Hz
  0.1-Hz to 10-Hz Noise: 0.25 μV_{PP}
- Excellent DC Precision:
  PSRR: 142 dB
  CMRR: 146 dB
  Open-Loop Gain: 136 dB
- Gain Bandwidth: 2 MHz
- Quiescent Current: 475 μA (Maximum)
- Wide Supply Range: ±2 V to ±18 V
- Rail-to-Rail Output:
  Input Includes Negative Rail
- RFI Filtered Inputs
- *Micro*SIZE Packages

2 Applications

- Bridge Amplifiers
- Strain Gauges
- Test Equipment
- Transducer Applications
- Temperature Measurement
- Electronic Scales
- Medical Instrumentation
- Resistance Temperature Detectors
- Precision Active Filters

3 Description

The OPA4188 operational amplifier uses TI proprietary auto-zeroing techniques to provide low offset voltage (25 μV, maximum), and near zero-drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 15 mV of the rails, making them ideal for industrial applications. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4 V to 36 V (±2 V to ±18 V).

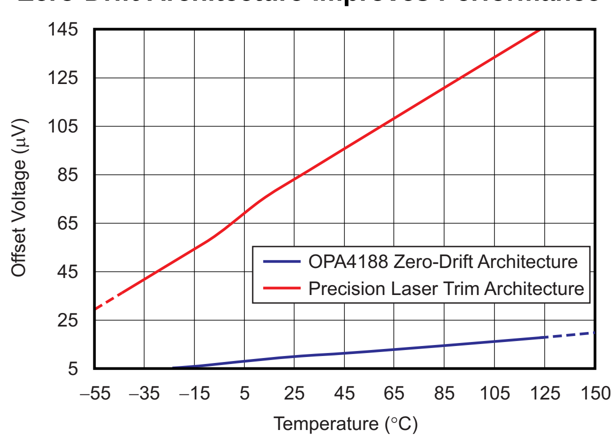
The quad version is available in 14-pin SOIC and 14-pin TSSOP packages. All versions are specified for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA4188	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Zero-Drift Architecture Improves Performance



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2015) to Revision D — **Page**

- Changed high supply over-temperature input bias current limit in *High-Voltage Operation Electrical Characteristics* table 6
- Changed high supply noise units in *High-Operating Voltage Electrical Characteristics* table 6
- Changed high supply room-temperature quiescent current limit in *High-Voltage Operation Electrical Characteristics* table 7
- Changed high supply over-temperature quiescent current limit in *High-Voltage Operation Electrical Characteristics table* 7
- Changed low supply over-temperature input bias current limit in *Low-Voltage Operation Electrical Characteristics table* 7
- Changed low supply noise units for input voltage noise density parameter in *Low-Voltage Operation Electrical Characteristics* table 7
- Changed low supply room-temperature quiescent current limit in *Low-Voltage Operation Electrical Characteristics* table 8
- Changed low supply over-temperature quiescent current limit in *Low-Voltage Operation Electrical Characteristics* table 8

Changes from Revision A (September 2012) to Revision B — **Page**

- Changed maximum specification of second Input Bias Current, I_B parameter row in *High-Voltage Operation Electrical Characteristics* table 6
- Changed maximum specification of second *Input Bias Current(I_B)* parameter in *Low-Voltage Electrical Characteristics* table 7
- Changed typical specifications for *Input impedance (Common-mode)* parameter in *Low-Voltage Electrical Characteristics* table 7

Changes from Original (June2012) to Revision A — **Page**

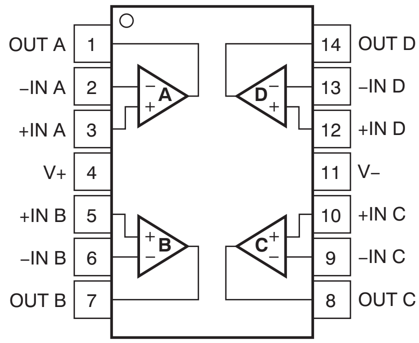
- Changed second to last *Applications* bullet 1

5 Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT (μV/°C)	BANDWIDTH (MHz)
Single	OPA188 (4 V to 36 V)	25	0.085	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4330 (5 V)	50	0.25	0.35

6 Pin Configuration and Functions

D or PW Packages
14-Pin SOIC or 14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output channel A
2	–IN A	I	Inverting input channel A
3	+IN A	I	Noninverting input channel A
4	V+	I	Positive power supply
5	+IN B	I	Noninverting input channel B
6	–IN B	I	Inverting input channel B
7	OUT B	O	Output channel B
8	OUT C	O	Output channel C
9	–IN C	I	Inverting input channel C
10	+IN C	I	Noninverting input channel C
11	V–	I	Negative power supply
12	+IN D	I	Noninverting input channel D
13	–IN D	I	Inverting input channel D
14	OUT D	O	Output channel D

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		±20	40 (single supply)	V
Signal input terminals(2)	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		±10	mA
Output short circuit(3)		Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5-V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Power supply voltage, (V+)-(V–)	4 (±2)		36 (±18)	V
Ambient temperature, T_A	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA4188		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

7.5 Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		T_A = 25°C		6	25	µV
dV_{OS}/dT			T_A = –40°C to 125°C		0.03	0.085	µV/°C
PSRR	Power-supply rejection ratio		V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	µV/V
			V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to 125°C			0.3	µV/V
	Long-term stability				4[(1)]		µV
	Channel separation, DC				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		V_{CM} = V_S / 2		±160	±1400	pA
			T_A = –40°C to 125°C			±18	nA
I_{OS}	Input offset current				±320	±2800	pA
			T_A = –40°C to 125°C			±6	nA
NOISE							
e_n	Input voltage noise		f = 0.1 Hz to 10 Hz		0.25		$µV_{PP}$
e_n	Input voltage noise density		f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density		f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to 125°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio		(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V, T_A = –40°C to 125°C	120	126		dB
INPUT IMPEDANCE							
	Input impedance	Differential			100 || 6		MΩ || pF
		Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	130	136		dB
			(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to 125°C	118	126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				2		MHz
SR	Slew rate		G = 1		0.8		V/µs
t_s	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		20		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		27		µs
	Overload recovery time		V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise		1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to 125°C		310	350	mV
I_{SC}	Short circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±4 V to V_S = ±18 V		415	500	µA
		I_O = 0 mA, T_A = –40°C to 125°C			570	µA
TEMPERATURE RANGE						
	Temperature range — Specified		–40		125	°C
	Temperature range — Operating		–55		150	°C
	Temperature range — Storage		–65		150	°C

7.6 Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		6	25	µV
dV_{OS}/dT		T_A = –40°C to 125°C		0.03	0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	µV/V
		V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to 125°C			0.3	µV/V
	Long-term stability			4(1)		µV
	Channel separation, DC			1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±1400	pA
		T_A = –40°C to 125°C			±18	nA
I_{OS}	Input offset current			±320	±2800	pA
		T_A = –40°C to 125°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density	f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V, T_A = –40°C to 125°C	108	120		dB
INPUT IMPEDANCE						
	Input impedance — Differential			100 || 6		MΩ || pF
	Input impedance — Common-mode			6 || 9.5		10^{12} Ω || pF

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	120	130		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to 125°C	110	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = 1		0.8		V/µs
	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to 125°C		310	350	mV
I_{SC}	Short circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range			4 to 36 (±2 to ±18)		V
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		385	465	µA
		I_O = 0 mA, T_A = –40°C to 125°C			540	µA
TEMPERATURE RANGE						
	Temperature range, Specified		–40		125	°C
	Temperature range, Operating		–40		125	°C
	Temperature range, Storage		–65		150	°C

7.7 Typical Characteristics

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 10
CMRR vs Temperature	Figure 11, Figure 12
PSRR vs Temperature	Figure 13
0.1-Hz to 10-Hz Noise	Figure 14
Input Voltage Noise Spectral Density vs Frequency	Figure 15
THD+N Ratio vs Frequency	Figure 16
THD+N vs Output Amplitude	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Quiescent Current vs Temperature	Figure 19
Open-Loop Gain and Phase vs Frequency	Figure 20
Closed-Loop Gain vs Frequency	Figure 21
Open-Loop Gain vs Temperature	Figure 22
Open-Loop Output Impedance vs Frequency	Figure 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31, Figure 32
Large-Signal Settling Time (10-V Positive Step)	Figure 33
Large-Signal Settling Time (10-V Negative Step)	Figure 34
Short Circuit Current vs Temperature	Figure 35
Maximum Output Voltage vs Frequency	Figure 36
Channel Separation vs Frequency	Figure 37
EMIRR IN+ vs Frequency	Figure 38

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

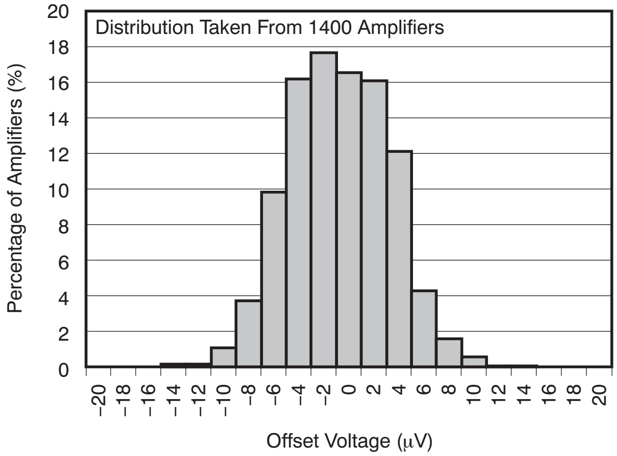


Figure 1. Offset Voltage Production Distribution

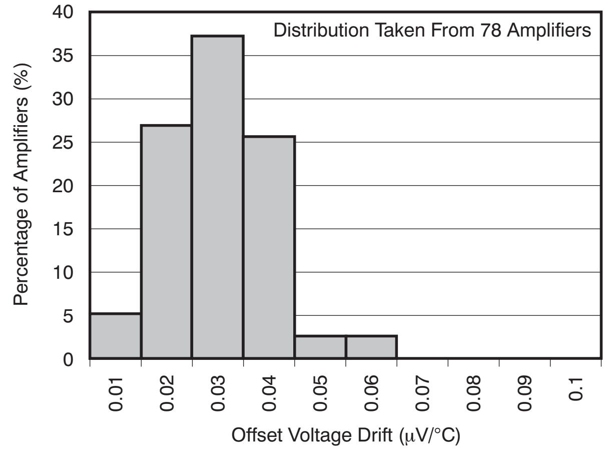


Figure 2. Offset Voltage Drift Distribution

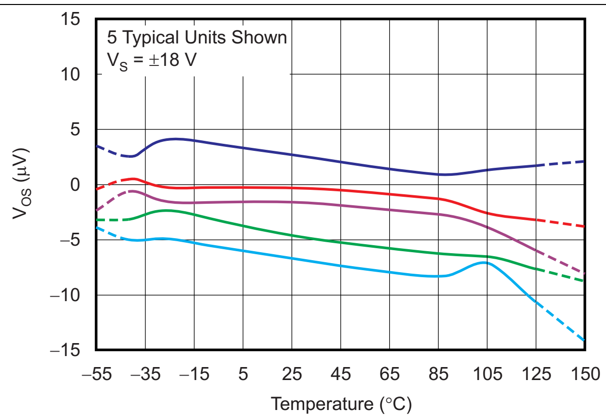


Figure 3. Offset Voltage vs Temperature

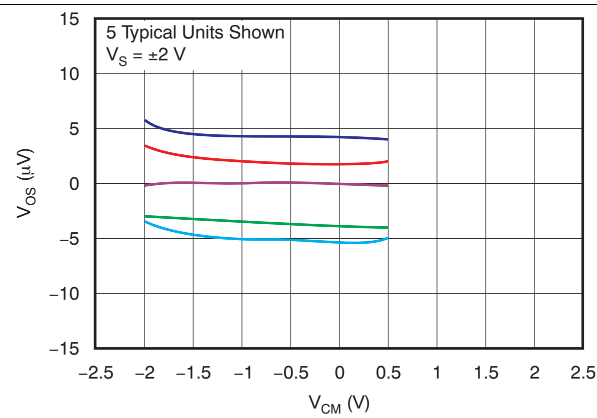


Figure 4. Offset Voltage vs Common-Mode Voltage

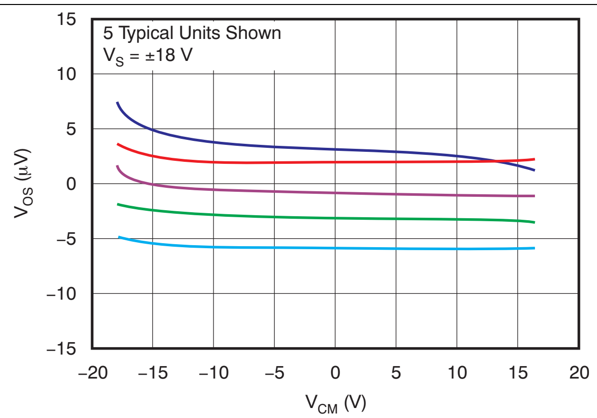


Figure 5. Offset Voltage vs Common-Mode Voltage

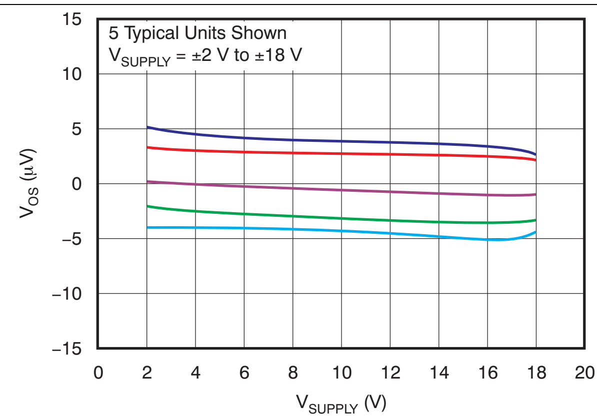


Figure 6. Offset Voltage vs Power Supply

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

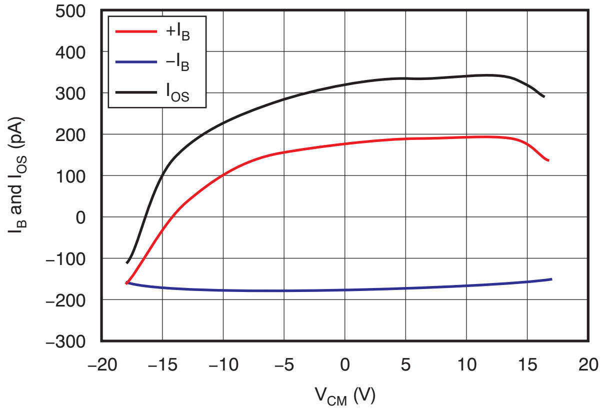


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

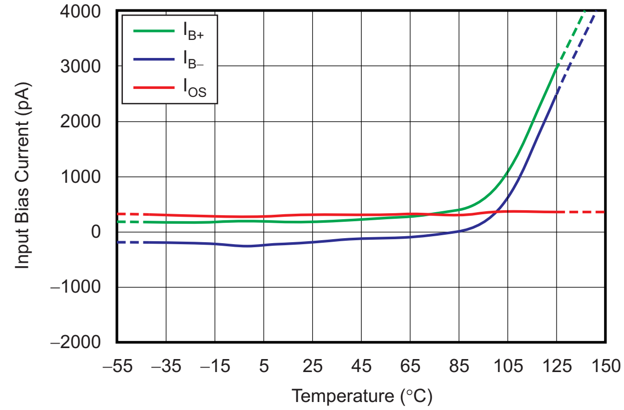


Figure 8. Input Bias Current vs Temperature

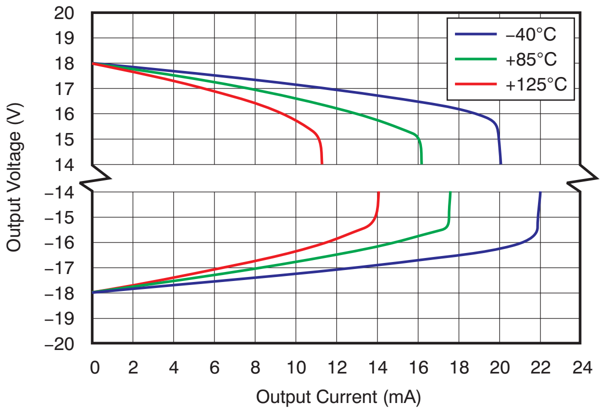


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

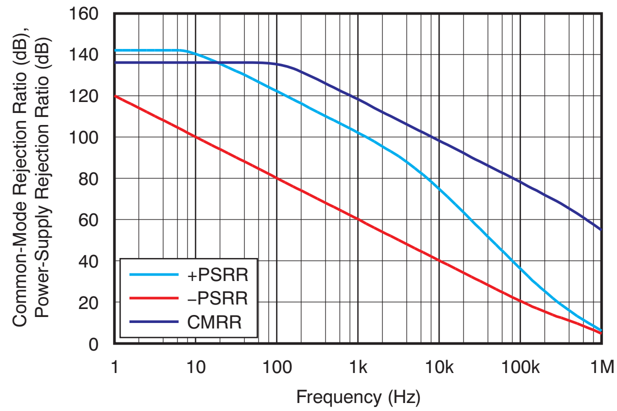


Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)

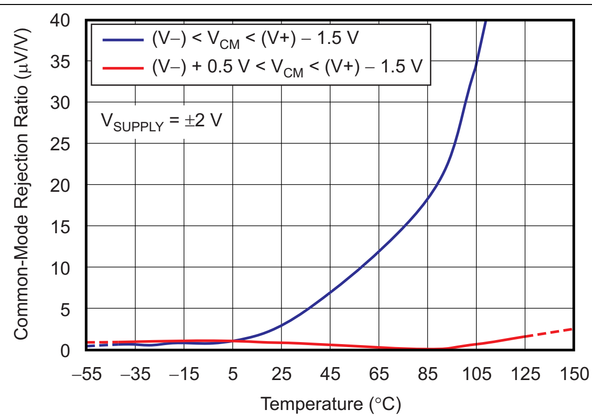


Figure 11. CMRR vs Temperature

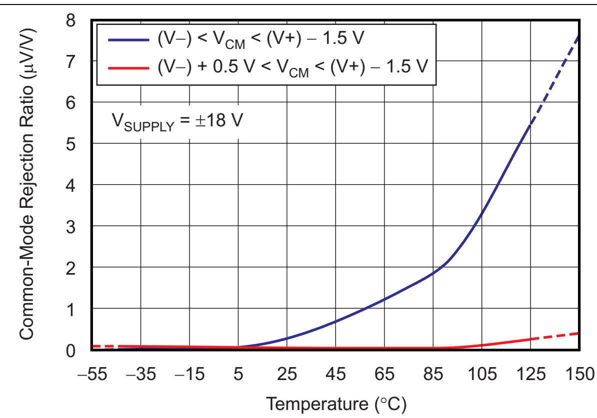


Figure 12. CMRR vs Temperature

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

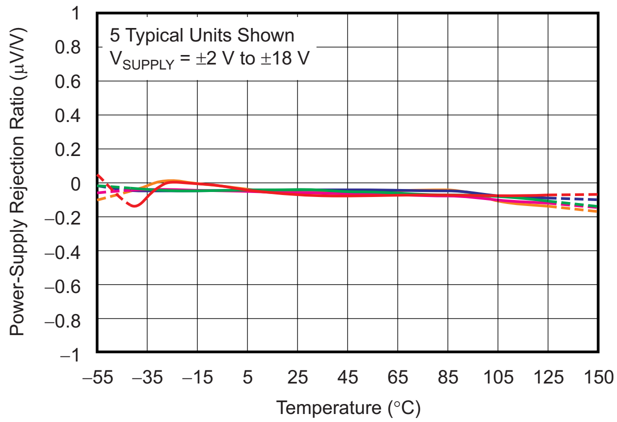


Figure 13. PSRR vs Temperature

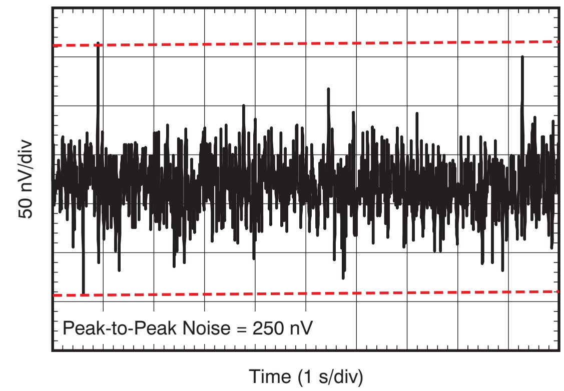


Figure 14. 0.1-Hz to 10-Hz Noise

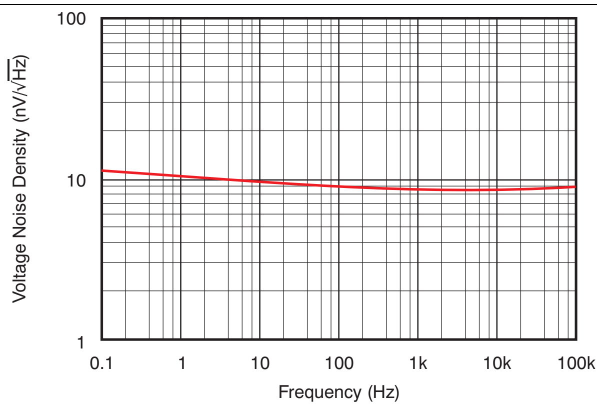


Figure 15. Input Voltage Noise Spectral Density vs Frequency

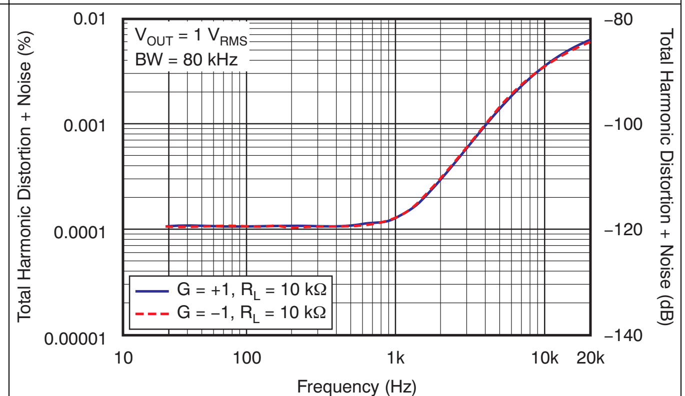


Figure 16. THD+N Ratio vs Frequency

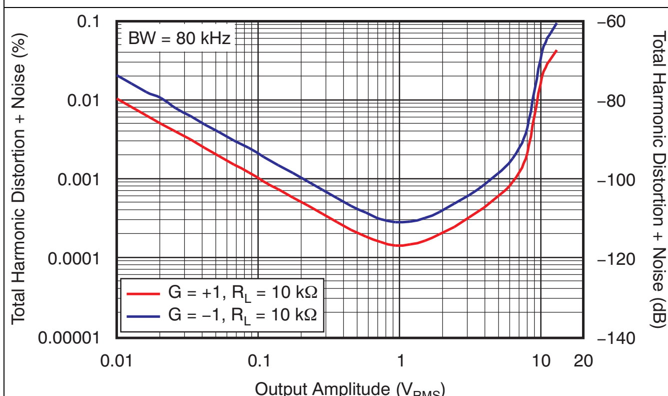


Figure 17. THD+N vs Output Amplitude

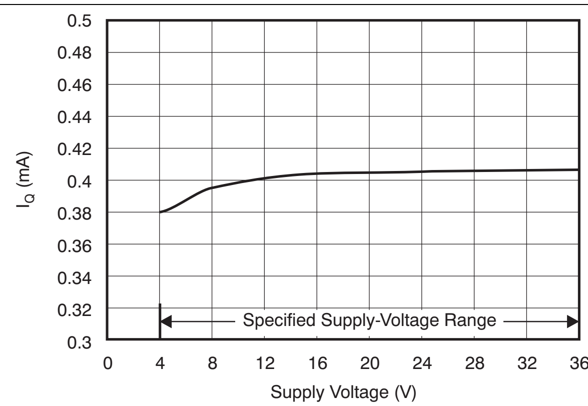


Figure 18. Quiescent Current vs Supply Voltage

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

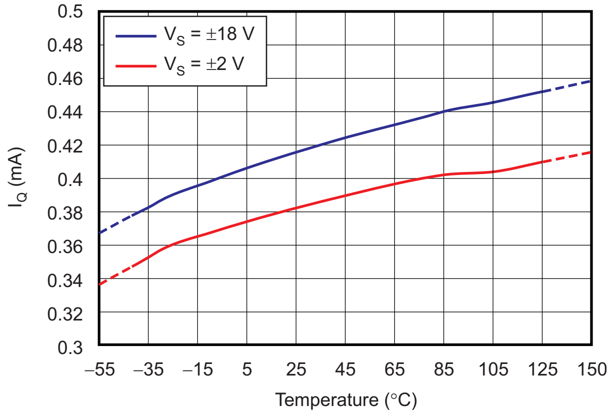


Figure 19. Quiescent Current vs Temperature

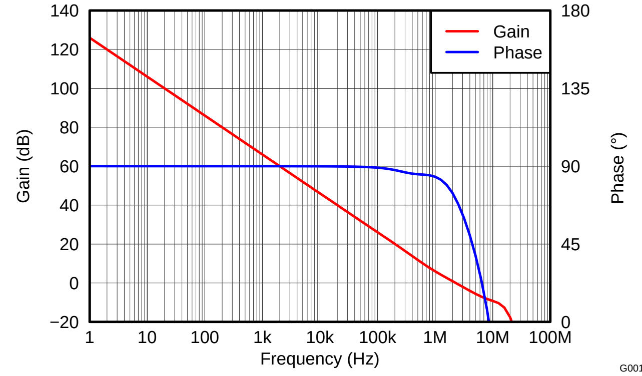


Figure 20. Open-Loop Gain and Phase vs Frequency

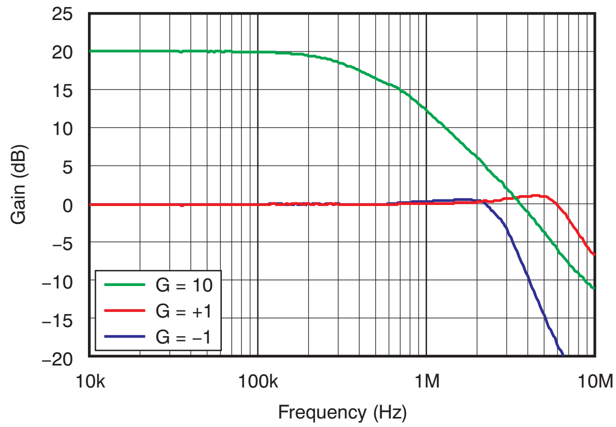


Figure 21. Closed-Loop Gain vs Frequency

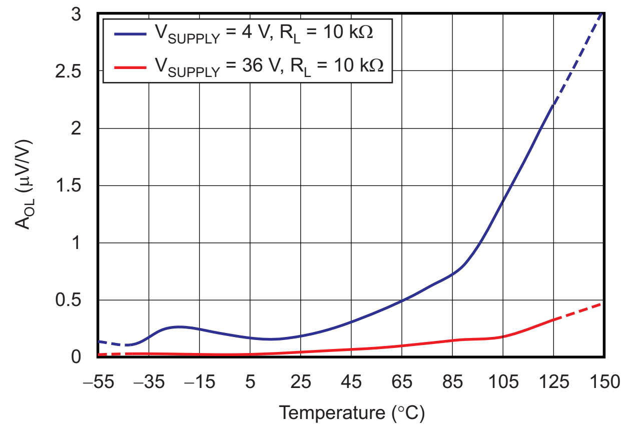


Figure 22. Open-Loop Gain vs Temperature

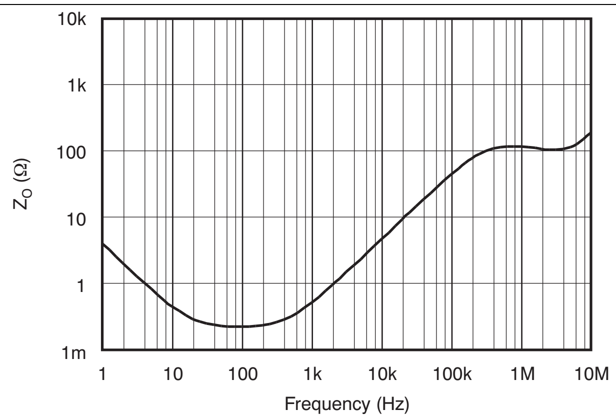


Figure 23. Open-Loop Output Impedance vs Frequency

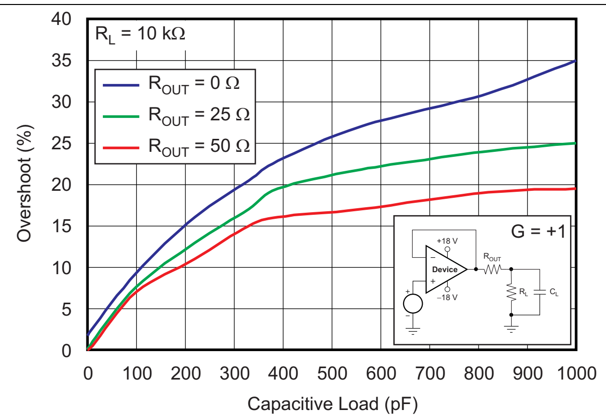


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

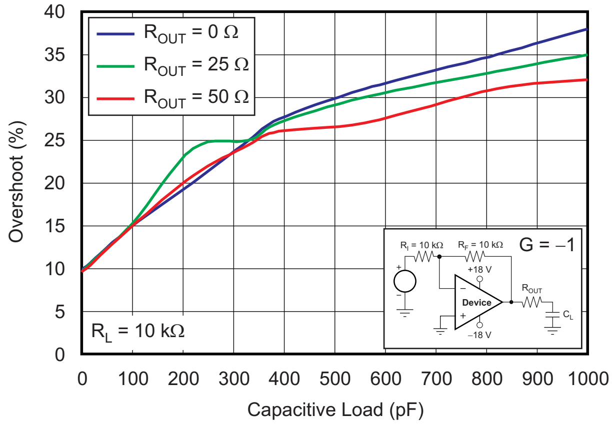


Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

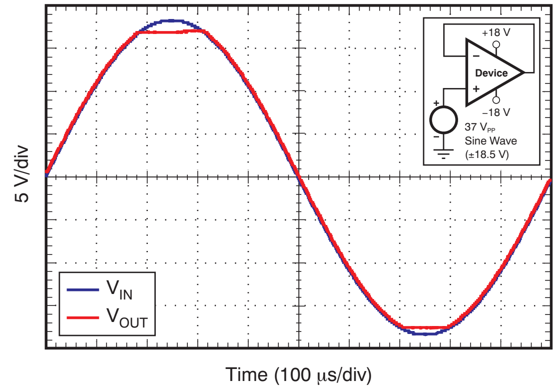


Figure 26. No Phase Reversal

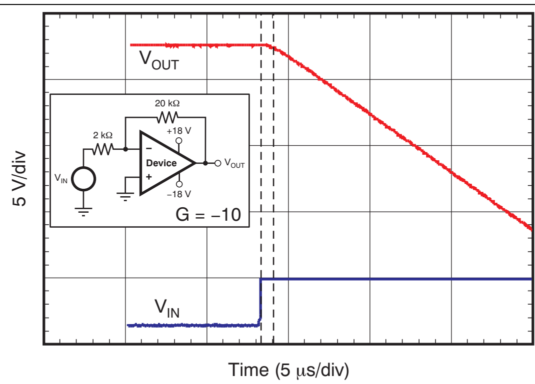


Figure 27. Positive Overload Recovery

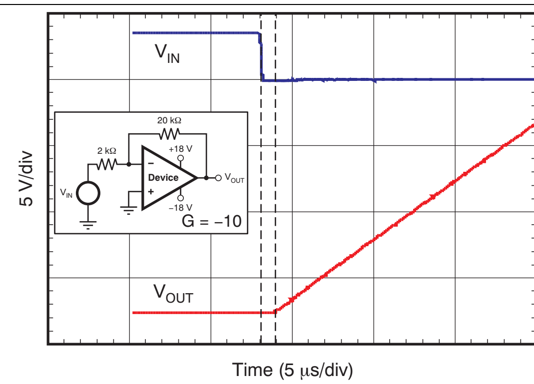


Figure 28. Negative Overload Recovery

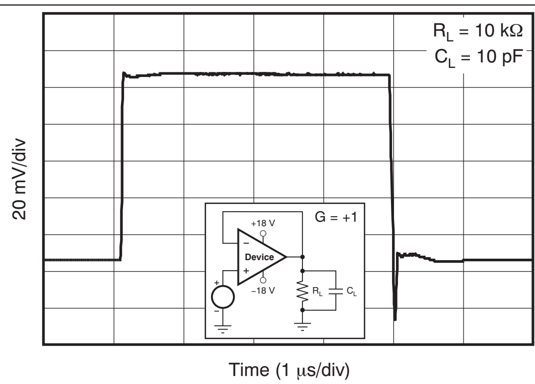


Figure 29. Small-Signal Step Response (100 mV)

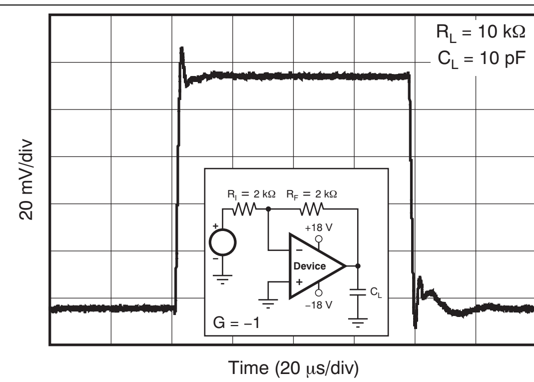


Figure 30. Small-Signal Step Response (100 mV)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

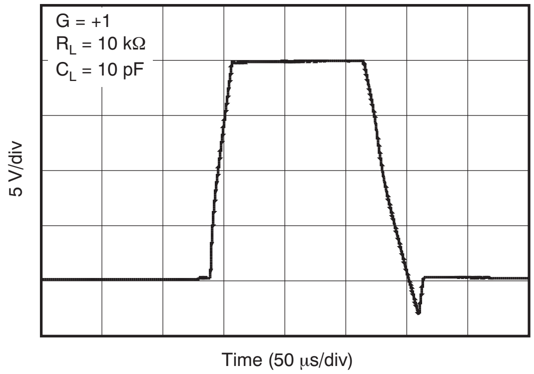


Figure 31. Large-Signal Step Response

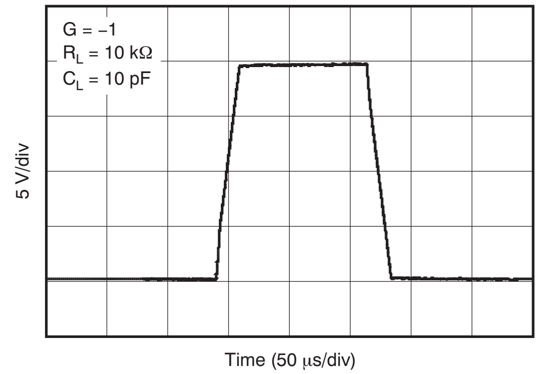


Figure 32. Large-Signal Step Response

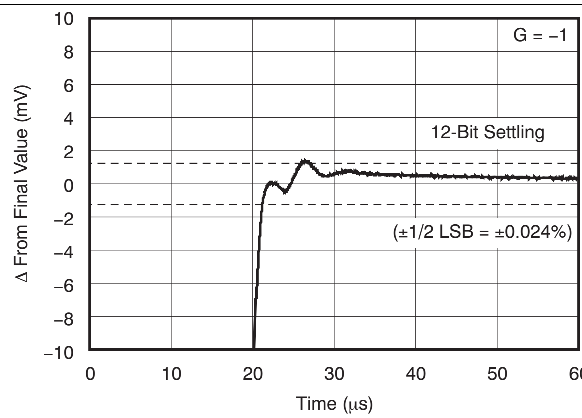


Figure 33. Large-Signal Settling Time (10-V Positive Step)

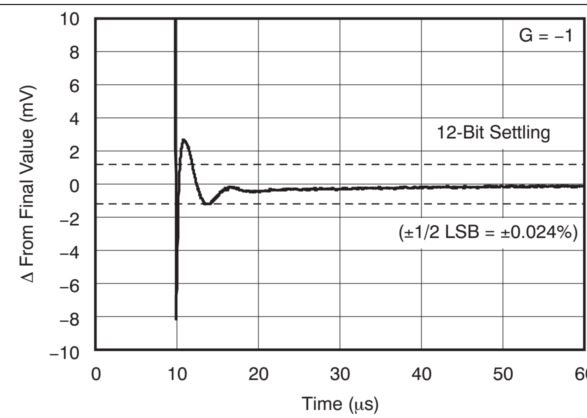


Figure 34. Large-Signal Settling Time (10-V Negative Step)

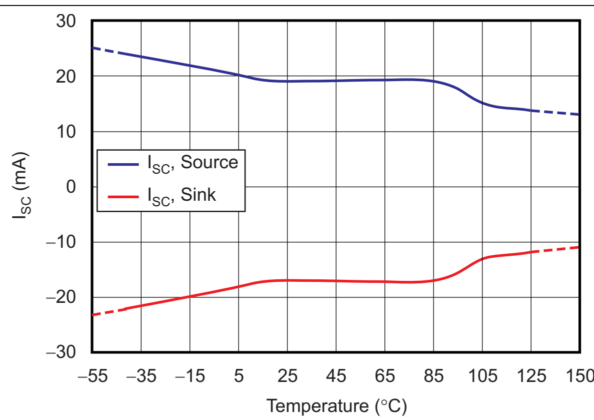


Figure 35. Short Circuit Current vs Temperature

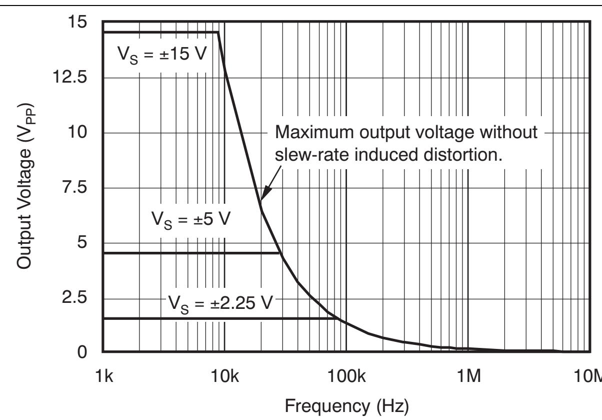


Figure 36. Maximum Output Voltage vs Frequency

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

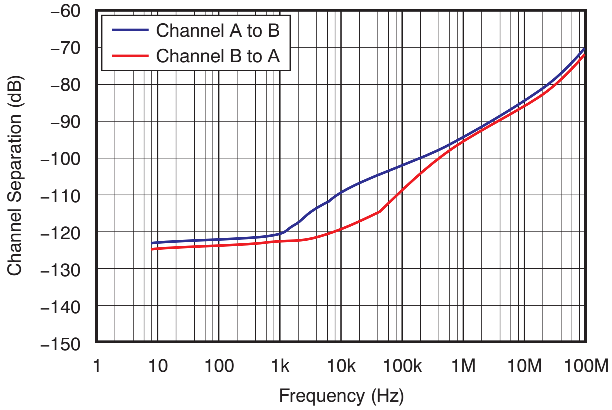


Figure 37. Channel Separation vs Frequency

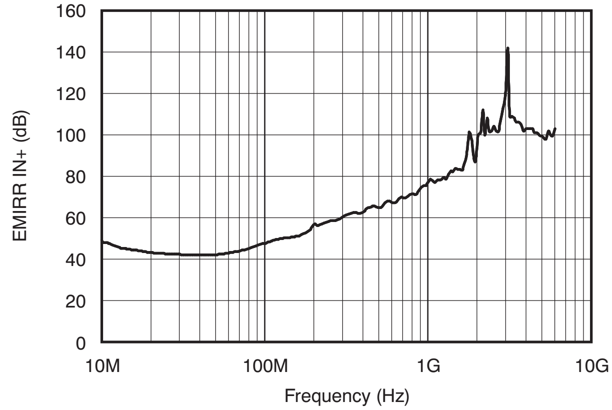


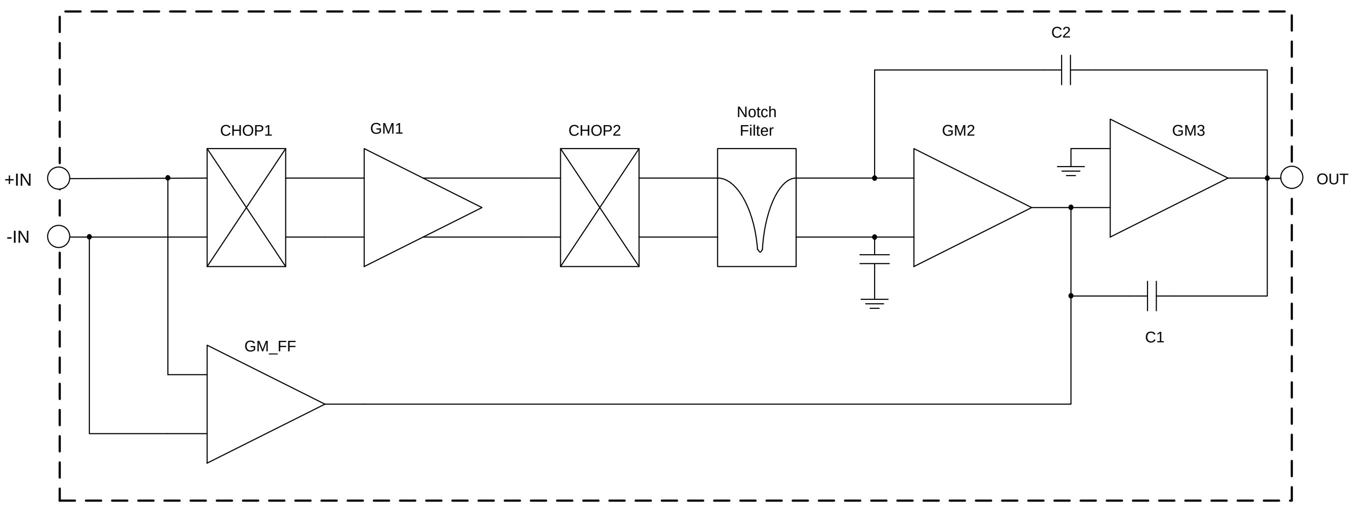
Figure 38. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPA4188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV per degree Celsius provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and AOL. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. The OPA4188 device is developed using TI's proprietary auto-zero architecture shown in *Functional Block Diagram*. The internal synchronous notch filter removes switching noise from the CHOP1 and CHOP2 stages, resulting in a low noise density of 8.8 nV/√Hz, low input offset voltage maximum of only 25 µV. Input offset drift maximum of only 0.085 µV/°C allows for calibration free system design.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Phase-Reversal Protection

The OPA4188 device has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA4188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 39.

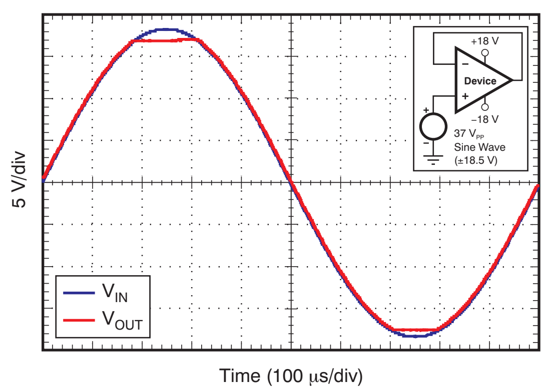


Figure 39. No Phase Reversal

Feature Description (continued)

8.3.2 Capacitive Load and Stability

The OPA4188 dynamic characteristics have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 40 and Figure 41 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com.

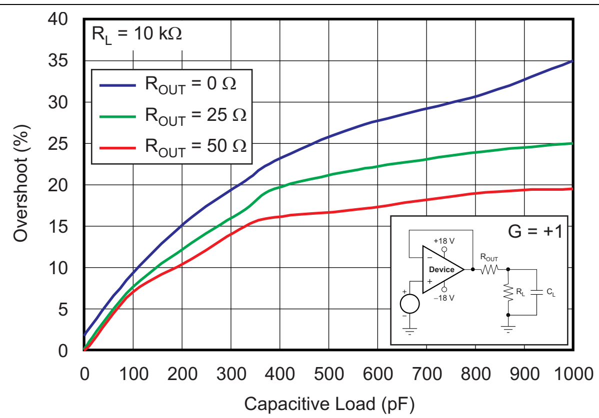


Figure 40. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

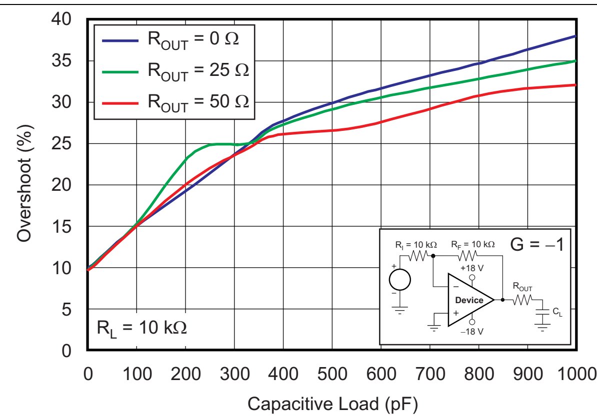


Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 42 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

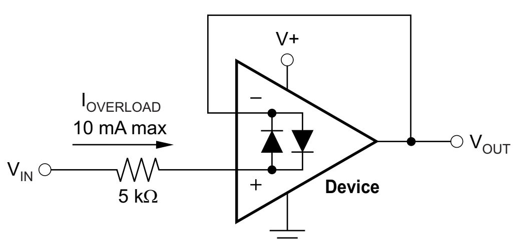


Figure 42. Input Current Protection

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

Feature Description (continued)

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.3.4 EMI Rejection

The OPA4188 device uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA4188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 43 shows the results of this testing on the OPA4188 device. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers* available for download from www.ti.com.

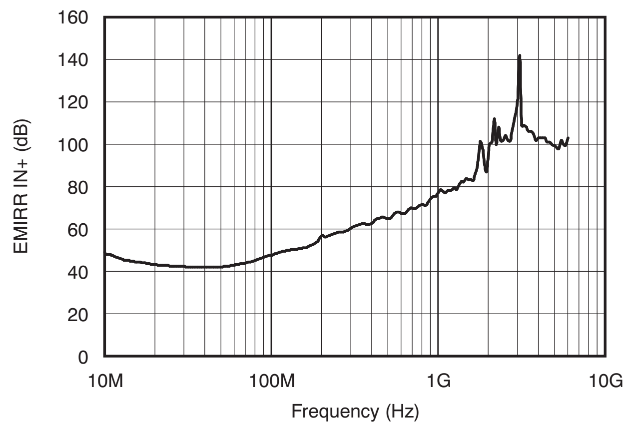


Figure 43. EMIRR Testing

8.4 Device Functional Modes

The OPA4188 device has a single functional mode that is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the OPA4188 is 36 V (±18 V).

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA4188 operational amplifier combines precision offset and drift with excellent overall performance, making it ideal for many precision applications. The precision offset drift of only 0.085 µV per degree Celsius provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The application examples of Figure 46 and Figure 47 highlight only a few of the circuits where the OPA4188 device can be used.

9.1.1 Operating Characteristics

The OPA4188 device is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

9.2 Typical Applications

9.2.1 Second Order Low Pass Filter

Low pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA4188 device is ideally suited to construct a high precision active filter. Figure 44 illustrates a second order low pass filter commonly encountered in signal processing applications.

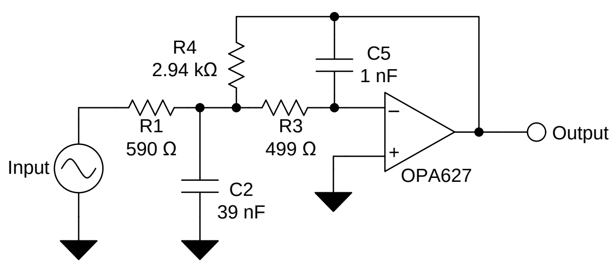


Figure 44. 25-kHz Low Pass Filter

9.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 44. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \tag{1}$$

Typical Applications (continued)

This circuit produces a signal inversion. For this circuit, use Equation 2 to calculate the gain at DC and the low-pass cutoff frequency.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{\left(1/R_3R_4C_2C_5\right)} \tag{2}$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

9.2.1.3 Application Curve

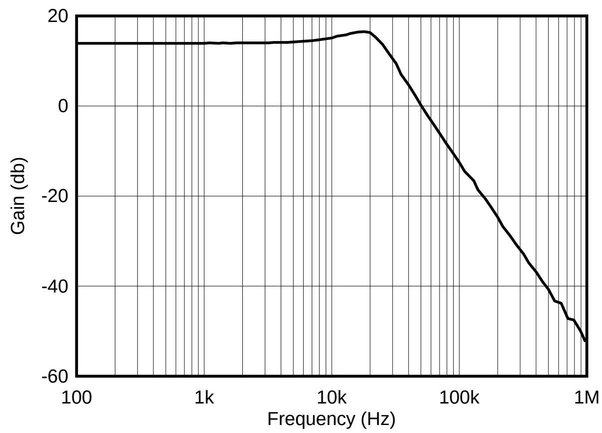


Figure 45. Gain (dB) vs Frequency (Hz)

9.2.2 Discrete INA + Attenuation for ADC With a 3.3-V Supply

Figure 46 illustrates a circuit with high input impedance that can accommodate ±2 V differential input signals. The output, V_{OUT}, is scaled into the full scale input range of a 3.3 V analog to digital converter. Input common mode voltages as high as ±10 V can be present with no signal clipping. Input stage gain is determined by resistors R_5, R_G and R_7 according to Equation 3 .

$$\text{Gain} = 0.2\text{x}\frac{\left(R_5 + R_7\right)}{R_G} \tag{3}$$

Typical Applications (continued)

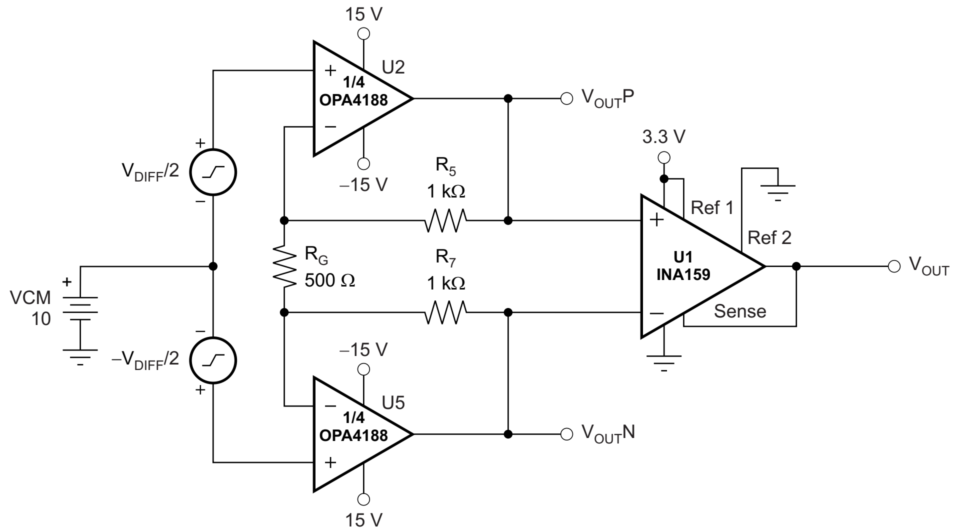
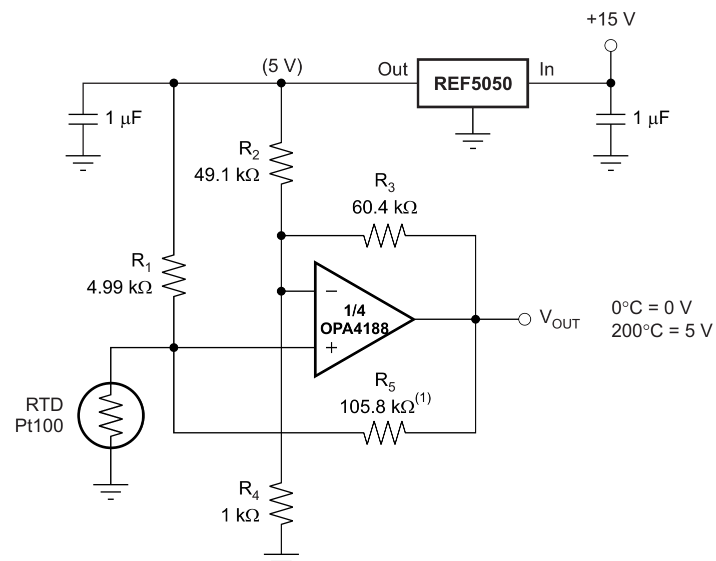


Figure 46. Discrete INA + Attenuation for ADC With a 3.3-V Supply Circuit

9.2.3 RTD Amplifier With Linearization

The OPA4188 device with ultra-low input offset voltage and ultra-low input offset voltage drift is ideally suited for RTD signal conditioning. Figure 47 illustrates a Pt100 RTD with excitation provided by a voltage reference and resistor R_1. Linearization is provided by R_5. Gain is determined by R_2, R_3 and R_4. The circuit is configured such that the output, V_{OUT}, ranges from 0 V to 5 V over the temperature range from 0°C to 200°C. The OPA4188 requires split power supplies (±5.35 V to ±15 V) for proper operation in this configuration.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 47. RTD Amplifier With Linearization Circuit

10 Power Supply Recommendations

The OPA4188 device is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 125°C and –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

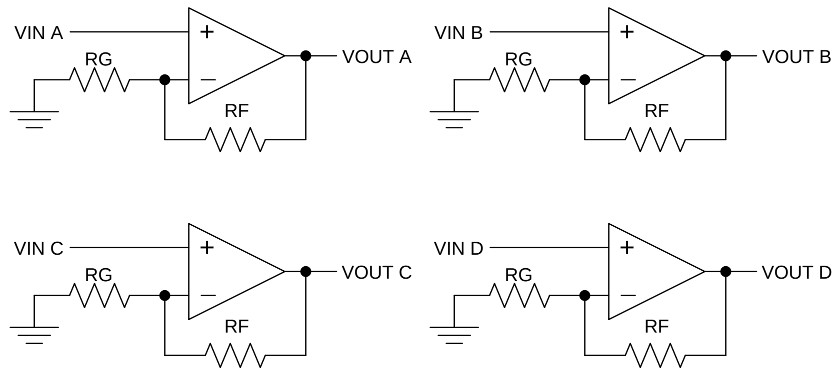
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The OPA6x7 is capable of high-output current (in excess of 45 mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1-µF solid tantalum capacitors may improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 48, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- The case (TO-99 metal package only) is internally connected to the negative power supply, as with most common operational amplifiers.
- Pin 8 of the plastic PDIP, SOIC, and TO-99 packages has no internal connection.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example



(Schematic Representation)

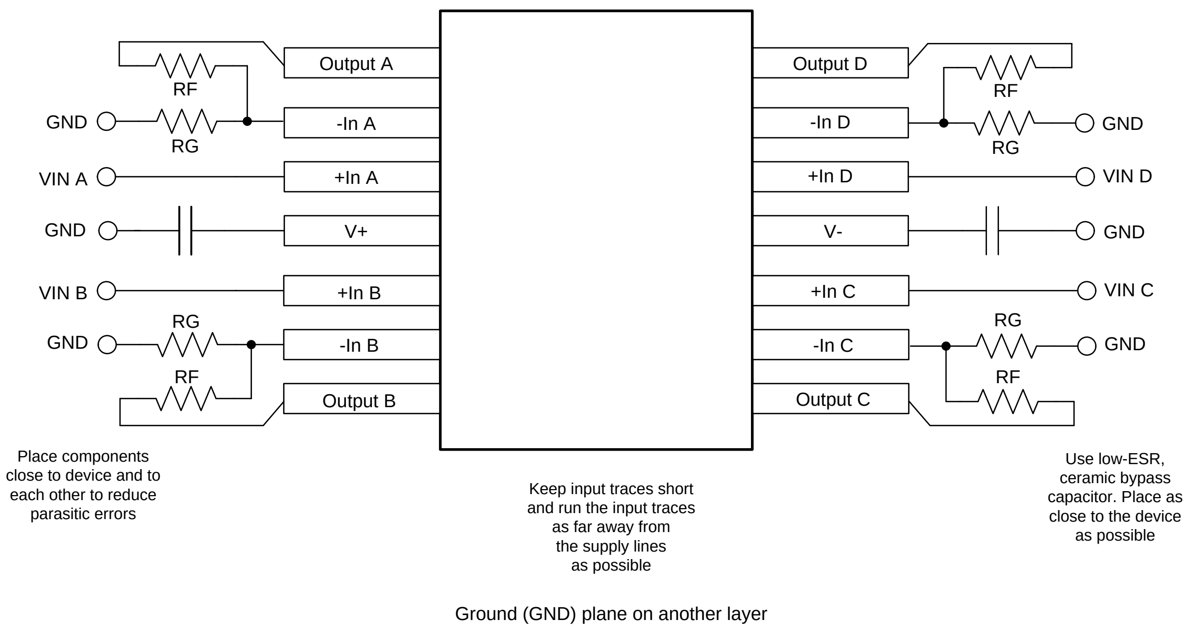


Figure 48. OPA4188 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Device Support

12.1.1.1 Development Support

12.1.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.1.2 TI Precision Designs

The OPAx188 devices (or similar operational amplifiers) are featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.1.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.1.2 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques* (SLOA089).
- *Op Amps for Everyone* (SLOD006).
- *Operational amplifier gain stability, Part 3: AC gain-error analysis* (SLYT383).
- *Operational amplifier gain stability, Part 2: DC gain-error analysis* (SLYT374).
- *Using infinite-gain, MFB filter topology in fully differential active filters* (SLYT343).
- *Op Amp Performance Analysis* (SBOA054).
- *Single-Supply Operation of Operational Amplifiers* (SBOA059).
- , *Tuning in Amplifiers* (SBOA067).
- *Shelf-Life Evaluation of Lead-Free Component Finishes* (SZZA046).

12.2 Trademarks

TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4188AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	Samples
OPA4188AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	Samples
OPA4188AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	Samples
OPA4188AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

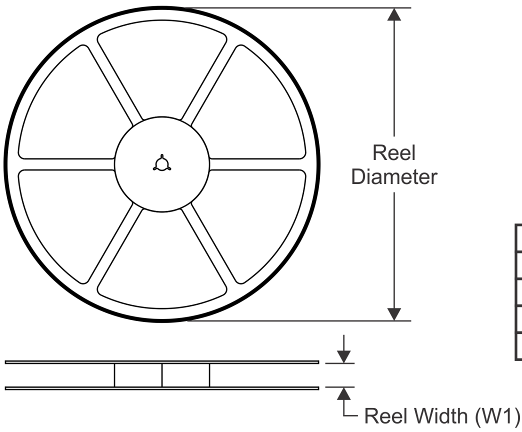
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

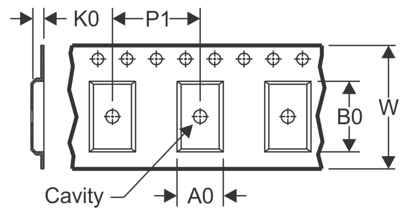
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

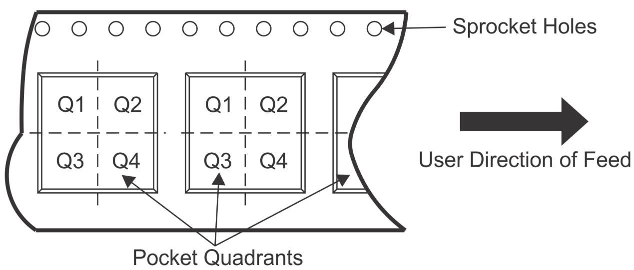


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

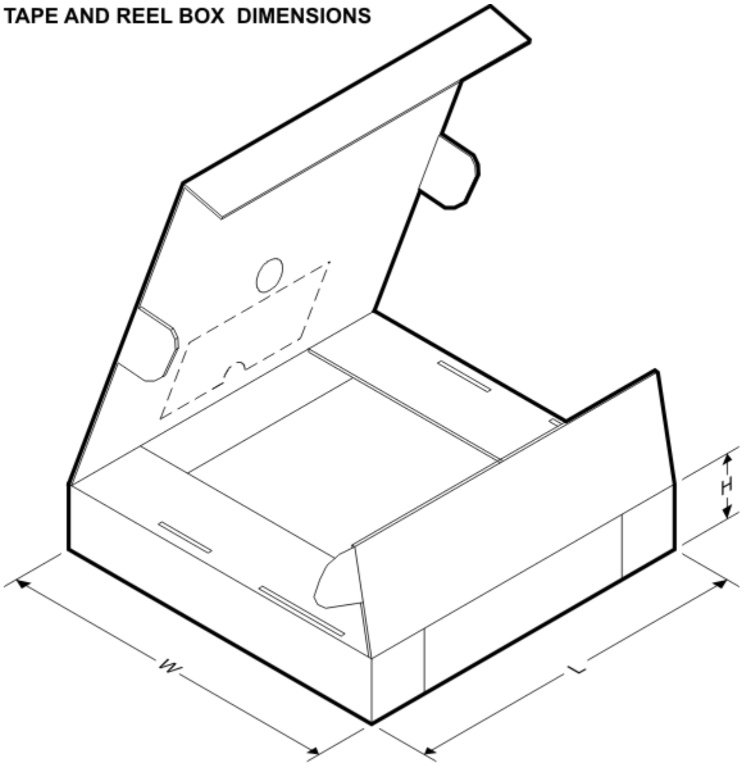
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4188AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4188AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

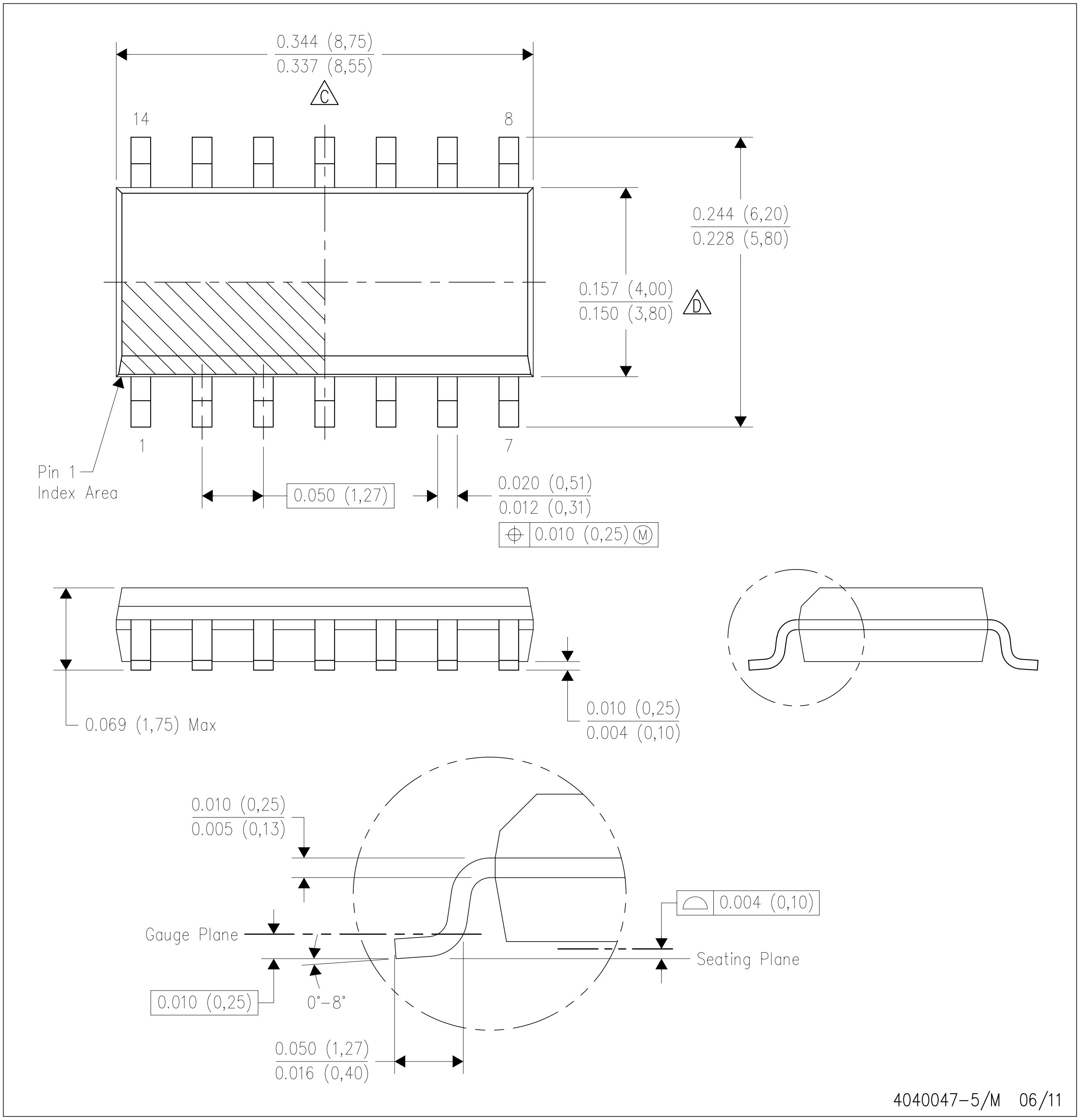
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

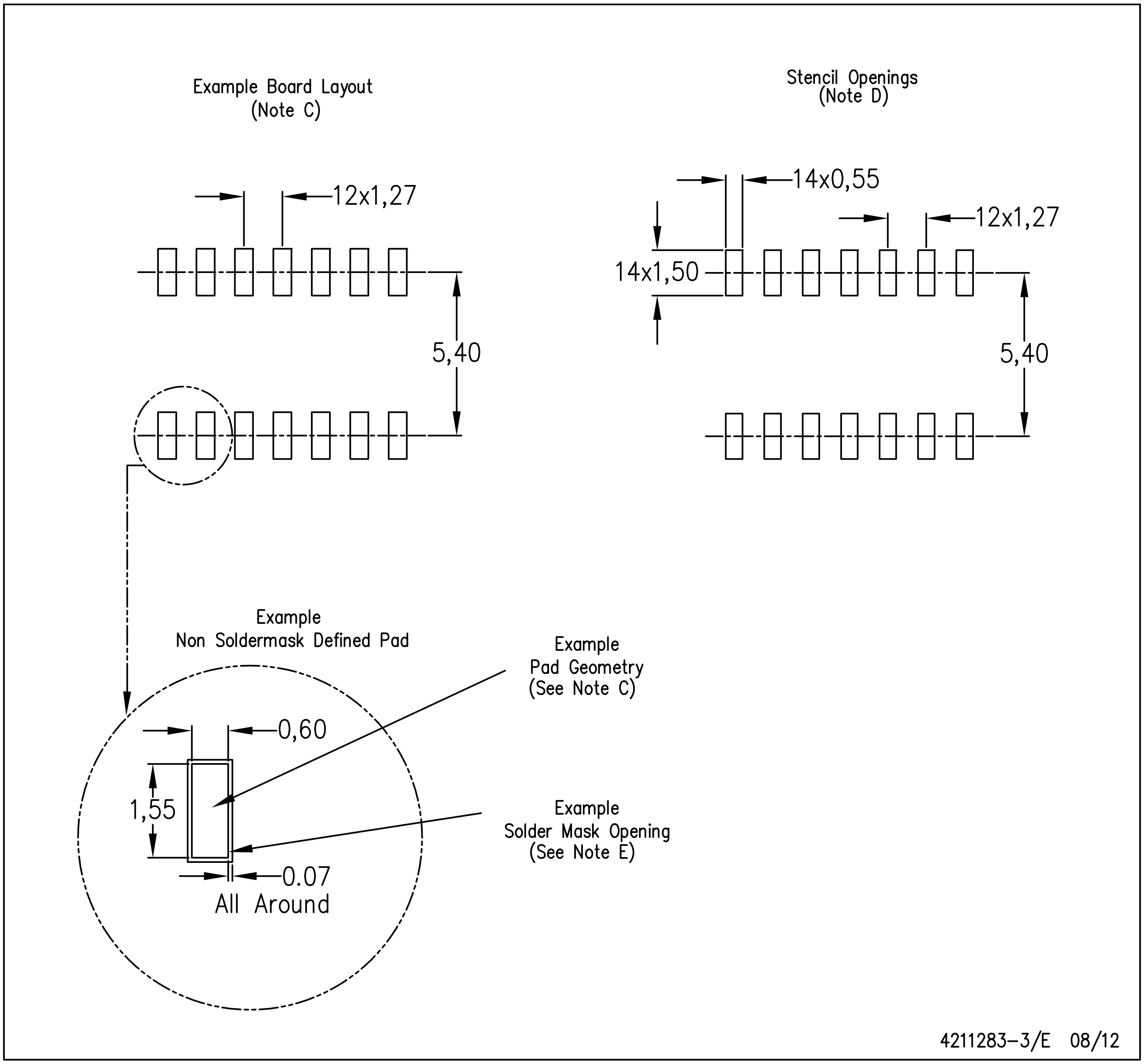
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4188AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4188AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



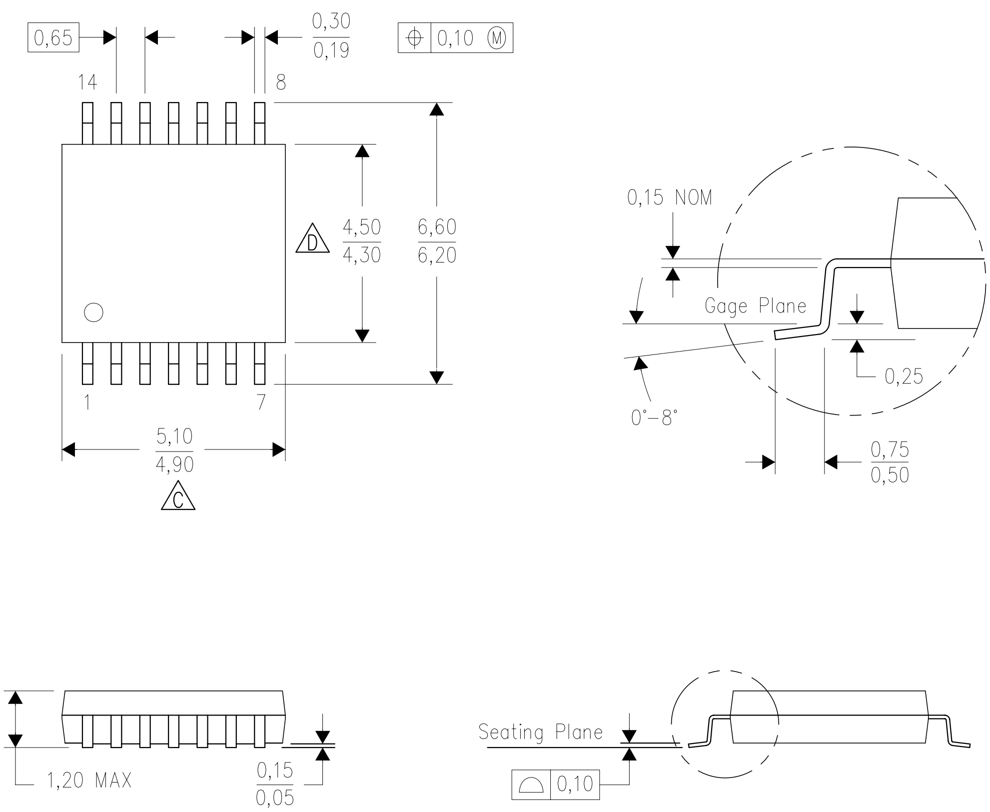
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

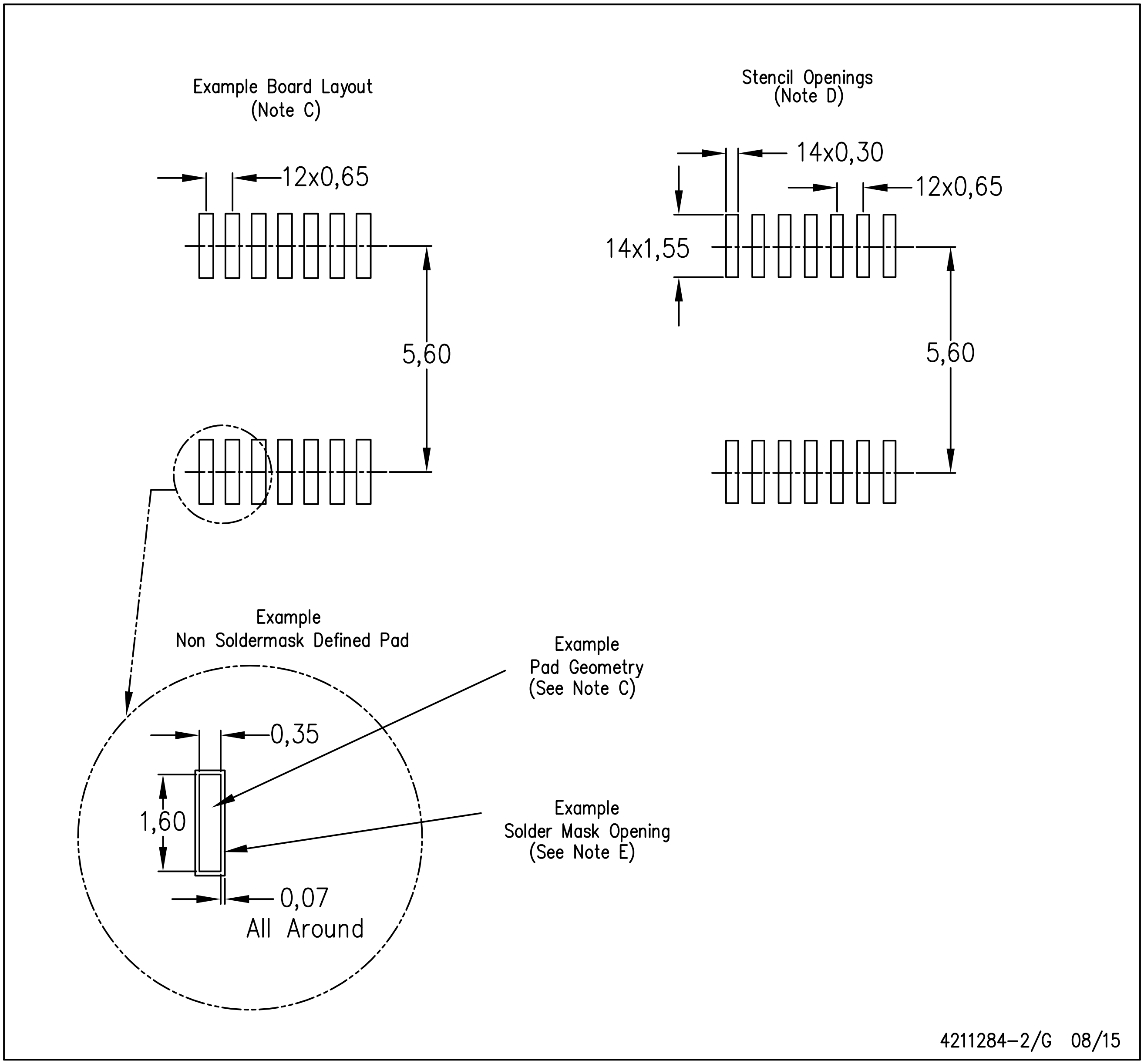
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.