



PSMN9R0-25MLC

N-channel 25 V 8.65 mΩ logic level MOSFET in LPAK33 using NextPower Technology

Rev. 3 — 15 June 2012

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

1.4 Quick reference data

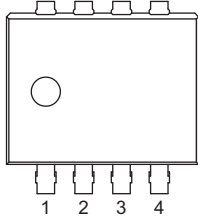
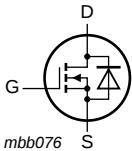
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C	-	-	25	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	55	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	45	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 15 A; T _j = 25 °C; see Figure 10	-	9.8	11.3	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see Figure 10	-	7.55	8.65	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 15 A; V _{DS} = 12.5 V; see Figure 12 ; see Figure 13	-	1.2	-	nC
Q _{G(tot)}	total gate charge	V _{GS} = 4.5 V; I _D = 15 A; V _{DS} = 12.5 V; see Figure 12 ; see Figure 13	-	5.4	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT1210 (LPAK33)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN9R0-25MLC	LPAK33	Plastic single ended surface mounted package (LPAK33); 4 leads	SOT1210

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25^\circ\text{C}$; see Figure 1	-	55	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100^\circ\text{C}$; see Figure 1	-	39	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$; see Figure 4	-	219	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; see Figure 2	-	45	W
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	120	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25^\circ\text{C}$	-	41	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$	-	219	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25^\circ\text{C}$; $I_D = 55\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; see Figure 3	-	8.7	mJ

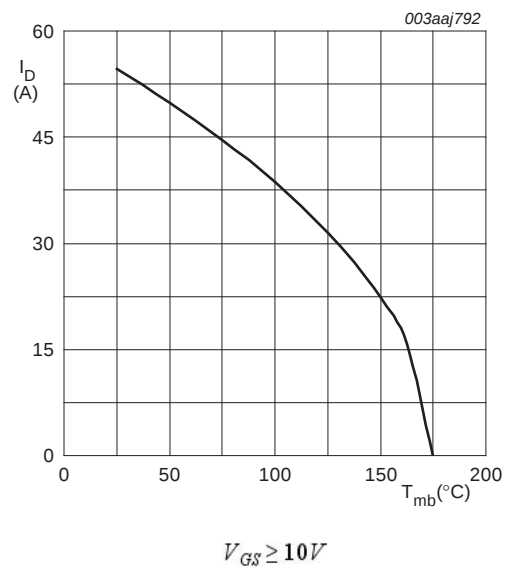


Fig 1. Continuous drain current as a function of mounting base temperature

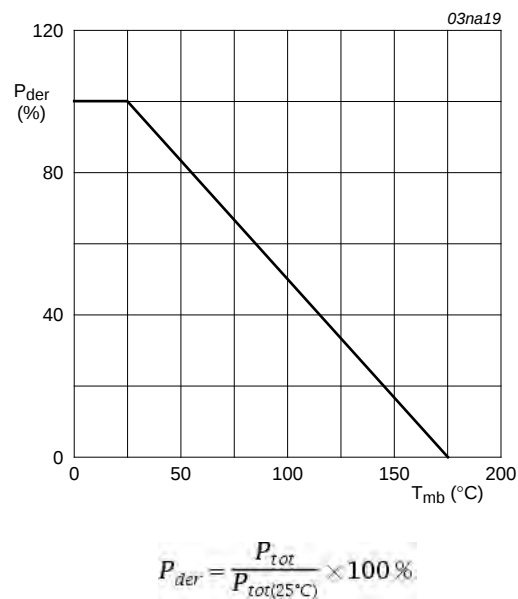


Fig 2. Normalized total power dissipation as a function of mounting base temperature

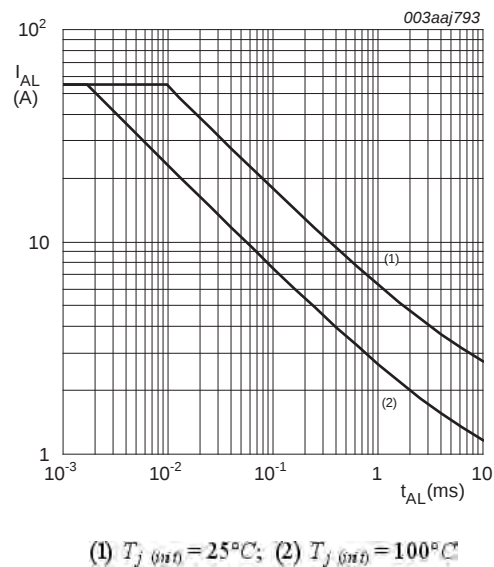
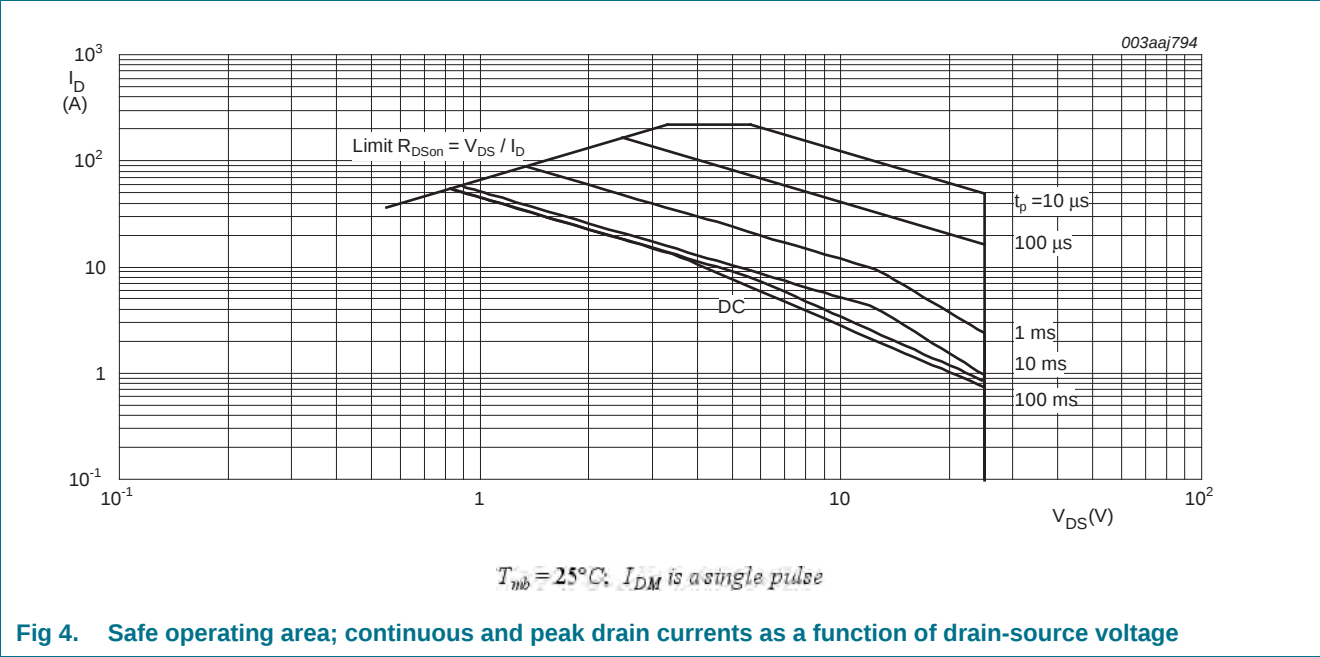


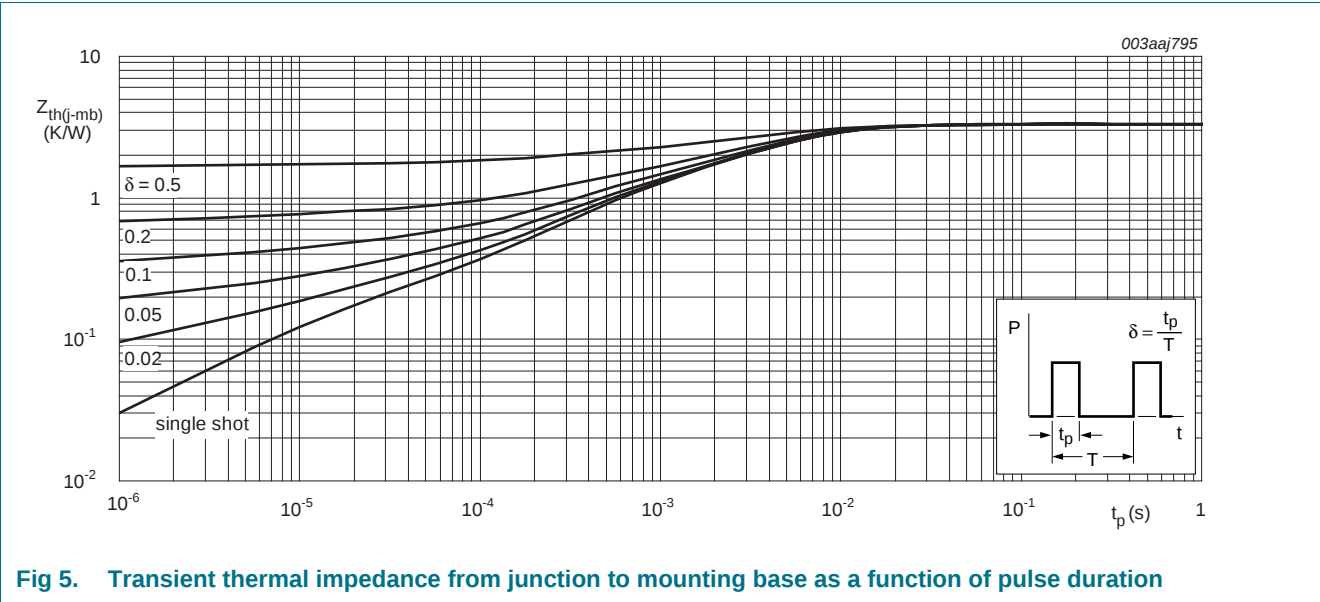
Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	3.1	3.32	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	25	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$	1.3	1.5	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-3.5	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	1	μA
		$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $T_j = 150\ ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 15\ A$; $T_j = 25\ ^\circ C$; see Figure 10	-	9.8	11.3	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 15\ A$; $T_j = 150\ ^\circ C$; see Figure 10 ; see Figure 11	-	-	18.1	mΩ
		$V_{GS} = 10\ V$; $I_D = 15\ A$; $T_j = 25\ ^\circ C$; see Figure 10	-	7.55	8.65	mΩ
		$V_{GS} = 10\ V$; $I_D = 15\ A$; $T_j = 150\ ^\circ C$; see Figure 10 ; see Figure 11	-	-	13.9	mΩ
R_G	gate resistance	$f = 1\ MHz$	0.95	1.9	3.8	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15\ A$; $V_{DS} = 12.5\ V$; $V_{GS} = 10\ V$; see Figure 12 ; see Figure 13	-	11.7	-	nC
		$I_D = 15\ A$; $V_{DS} = 12.5\ V$; $V_{GS} = 4.5\ V$; see Figure 12 ; see Figure 13	-	5.4	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	11.1	-	nC
Q_{GS}	gate-source charge	$I_D = 15\ A$; $V_{DS} = 12.5\ V$; $V_{GS} = 4.5\ V$; see Figure 12 ; see Figure 13	-	1.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.6	-	nC
Q_{GD}	gate-drain charge		-	1.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15\ A$; $V_{DS} = 12.5\ V$; see Figure 12 ; see Figure 13	-	2.5	-	V
C_{iss}	input capacitance	$V_{DS} = 12.5\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_j = 25\ ^\circ C$; see Figure 14	-	705	-	pF
C_{oss}	output capacitance		-	206	-	pF
C_{rss}	reverse transfer capacitance		-	67	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12.5\text{ V}; R_L = 0.8\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	7.1	-	ns
t_r	rise time		-	10.1	-	ns
$t_{d(off)}$	turn-off delay time		-	11.1	-	ns
t_f	fall time		-	6.1	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12.5\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	5.3	-	nC

Source-drain diode

V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 15	-	0.83	1.1	V
t_{rr}	reverse recovery time	$I_S = 15\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12.5\text{ V}$	-	14.8	-	ns
Q_r	recovered charge		-	7.5	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 15\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$ $V_{DS} = 12.5\text{ V};$ see Figure 16	-	8.9	-	ns
t_b	reverse recovery fall time		-	5.9	-	ns

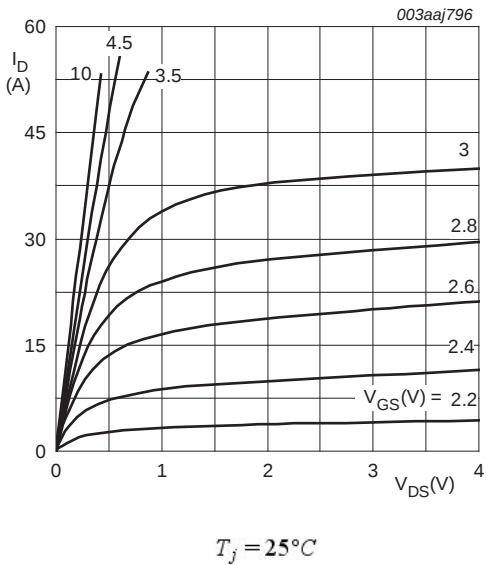


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

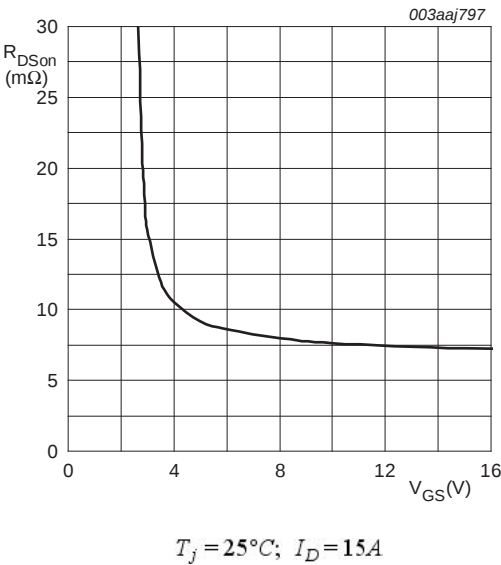


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

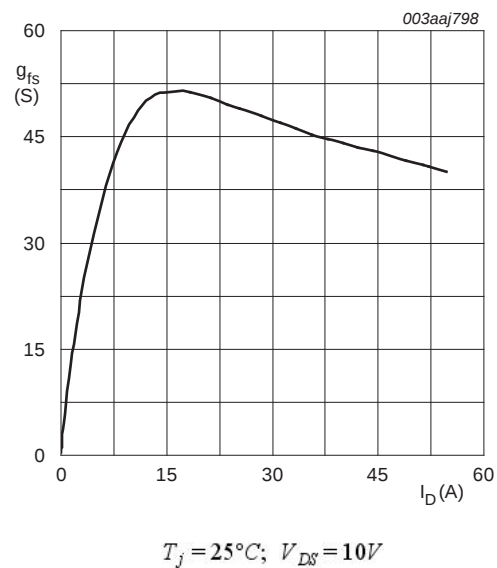


Fig 8. Forward transconductance as a function of drain current; typical values

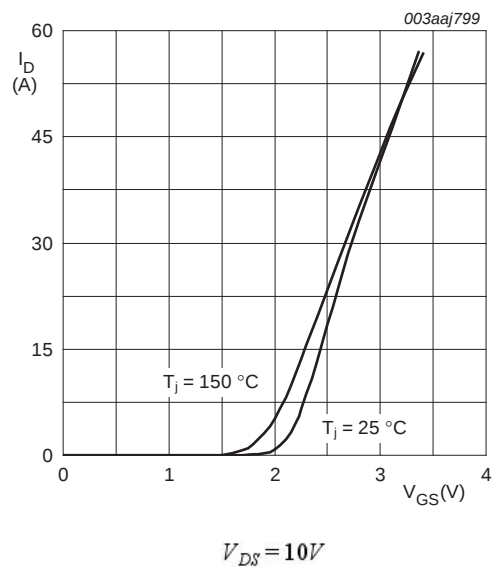


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

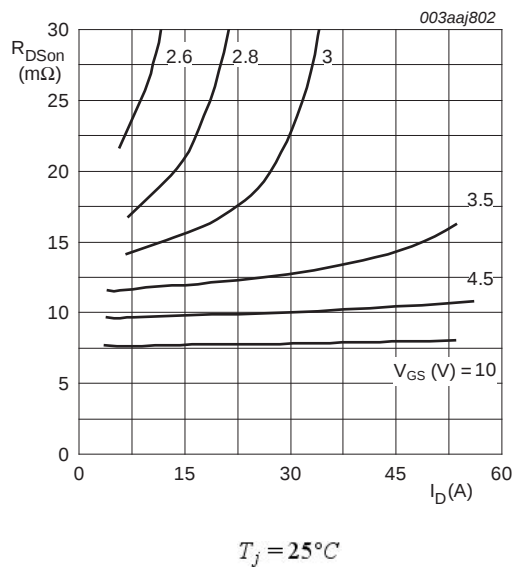


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

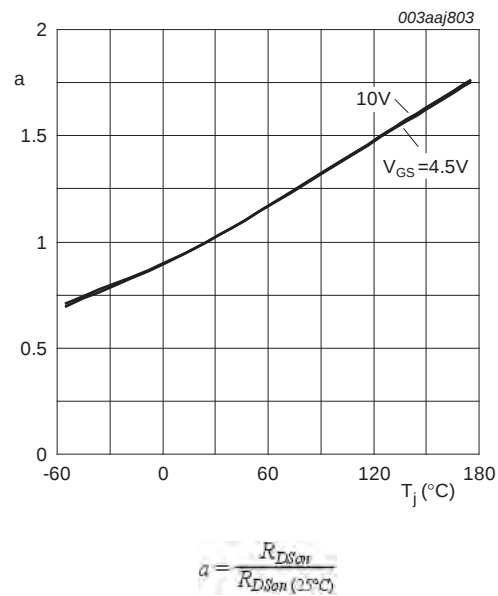
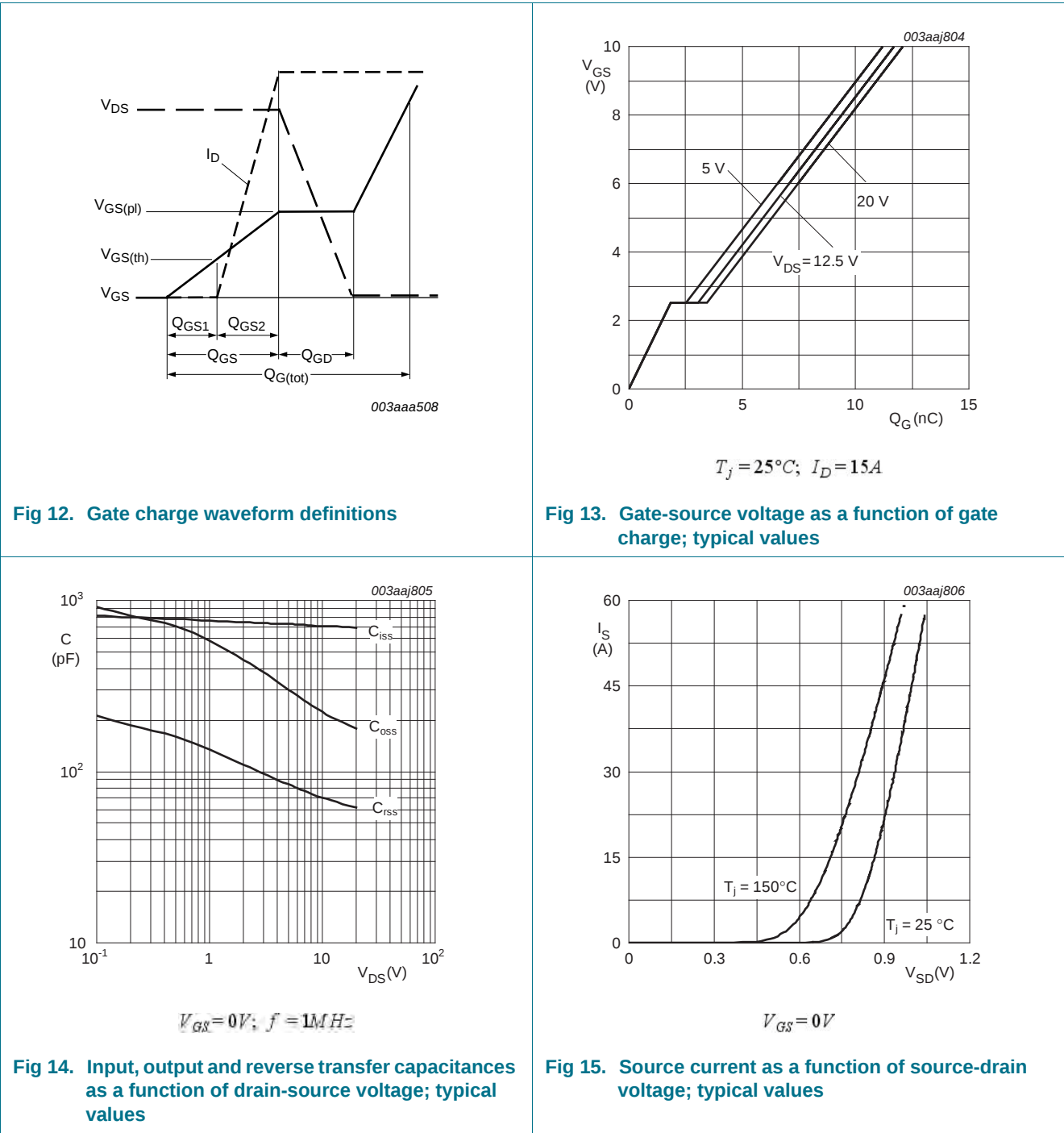


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



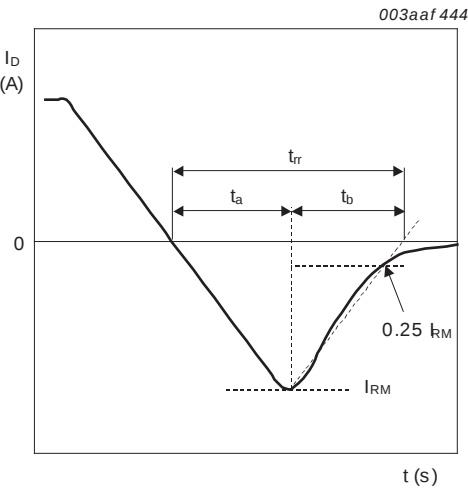
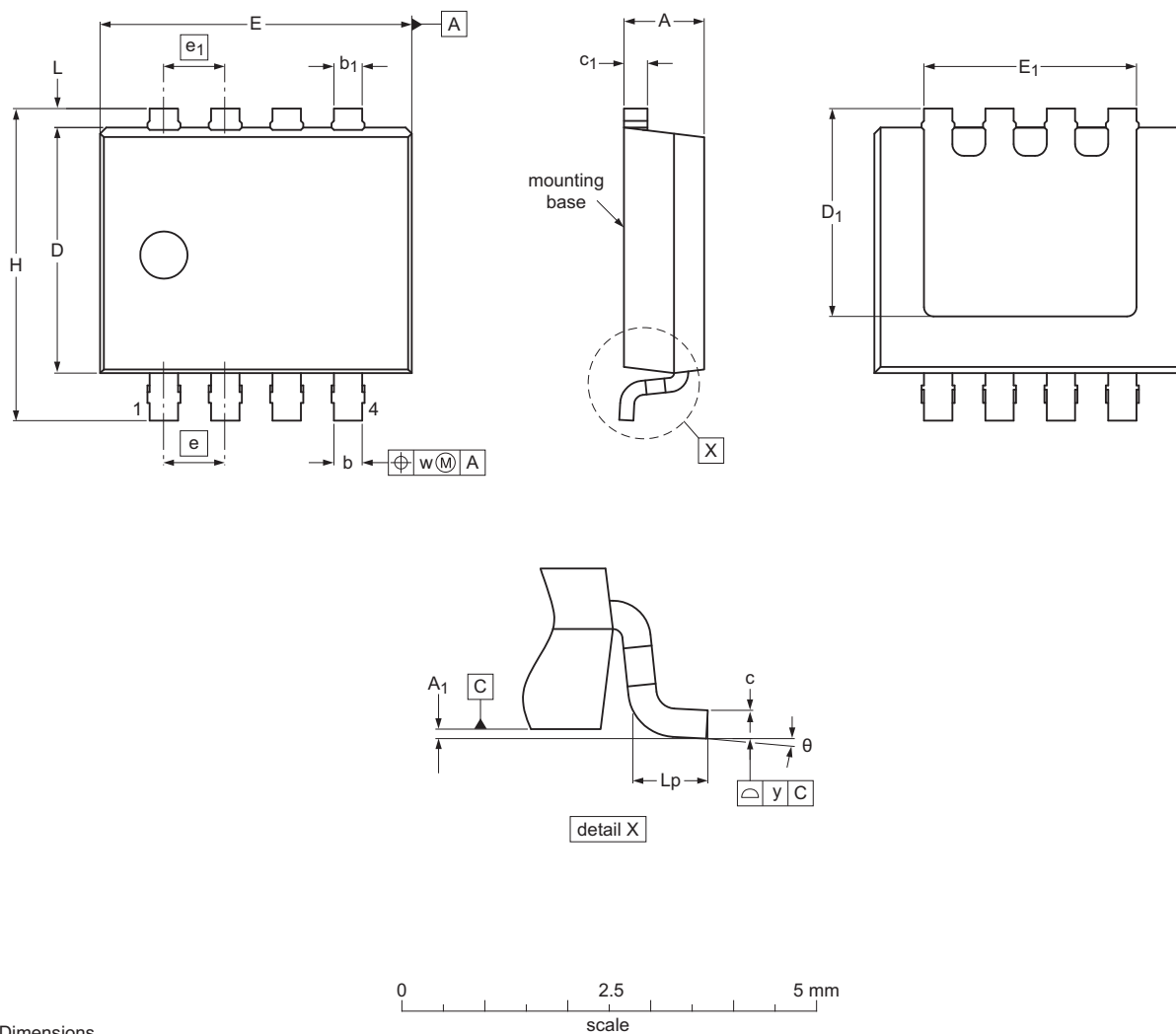


Fig 16. Reverse recovery timing definition

7. Package outline

Plastic single ended surface mounted package (LPAK33); 8 leads

SOT1210



Dimensions										scale									
Unit ⁽¹⁾	A	A ₁	b	b ₁	c	c ₁	D ⁽¹⁾	D ₁	E ⁽¹⁾	E ₁	e	e ₁	H	L	L _p	w	y	ε	
mm	max	0.90	0.10	0.35	0.35	0.20	0.30	2.70	2.35	3.40	2.45	0.65	0.65	3.40	0.25	0.50	0.20	0.10	8
	min	0.80	0.00	0.25	0.25	0.10	0.20	2.50	1.90	3.20	2.00			3.20	0.13	0.30			0

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210 po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						11-12-19 12-03-12

Fig 17. Package outline SOT1210 (LFAK33)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R0-25MLC v.3	20120615	Product data sheet	-	PSMN9R0-25MLC v.2
Modifications:	• Various changes to content.			
PSMN9R0-25MLC v.2	20120607	Product data sheet	-	PSMN9R0-25MLC v.1

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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Date of release: 15 June 2012

Document identifier: PSMN9R0-25MLC