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# Specification

## MCOB128064JS1V-YP



# 1.Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2011/02/28	1		First issue

# 2. General Specification

The Features is described as follow:

- Module dimension: 75.0 × 52.7 × 8.5 (max.) mm<sup>3</sup>
- View area: 57.01 × 29.49 mm<sup>2</sup>
- Active area: 53.73 × 26.85 mm<sup>2</sup>
- Number of dots: 128 x 64
- Pixel size: 0.40x0.40 mm<sup>2</sup>
- Pixel pitch: 0.43 x 0.43 mm<sup>2</sup>
- Duty: 1/64
- Emitting Color: Yellow

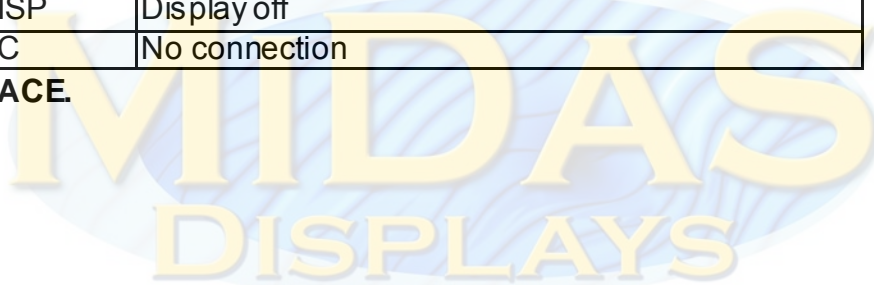
# Midas Displays OLED Part Number System

<b>MCO</b>	<b>B</b>	<b>21605</b>	<b>A</b>	<b>*</b>	<b>V</b>	<b>-</b>	<b>E</b>	<b>W</b>	<b>I</b>	<b>*</b>
<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>		<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>
1	=	<b>MCO:</b>	Midas Displays OLED							
2	=	<b>Blank:</b>	<b>B:</b> COB (Chip on Board) <b>T:</b> TAB (Taped Automated Bonding)							
3	=	<b>No of dots:</b>	(e.g. 240064 = 240 x 64 dots)				(e.g. 21605 = 2 x 16 5mm C.H.)			
4	=	<b>Series</b>	A to Z							
5	=	<b>Series Variant:</b>	A to Z and 1 to 9 – see addendum							
6	=	<b>Operating Temp Range:</b>	<b>A:</b> -30+85° C		<b>V:</b> -40+80° C		<b>Y:</b> -40 +70° C		<b>Z:</b> -30+70° C	
			<b>X:</b> -40 +85° C							
7	=	<b>Character Set:</b>	<b>Blank:</b> Not Applicable							
			<b>E:</b> Multi European Font Set (English/Japanese – Western European (K) – Cyrillic (R))							
8	=	<b>Colour:</b>	<b>Y:</b> Yellow		<b>W:</b> White		<b>B:</b> Blue		<b>R:</b> Red	
			<b>G:</b> Green		<b>RGB:</b> Full Colour					
9	=	<b>Interface:</b>	<b>P:</b> Parallel		<b>I:</b> I <sup>2</sup> C		<b>S:</b> SPI		<b>M:</b> Multi	
10	=	<b>Voltage Variant:</b>	e.g. <b>3</b> = 3v							

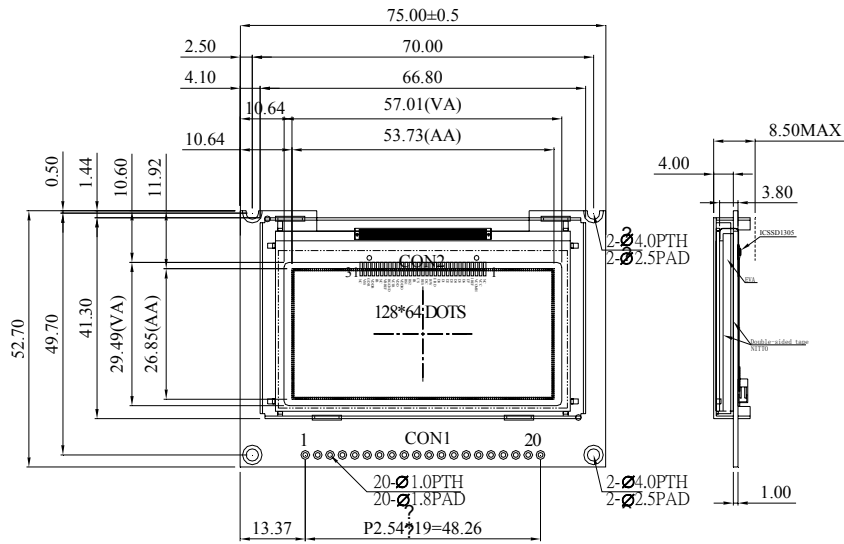
## 4. Interface Pin Function

No.	Symbol	Function
1	VDD	Power supply for analog circuit.
2	VSS	Ground.
3	NC	No connection
4~11	D0~D7	Data bus.
12	CS#	Chip select input.
13	NC	No connection
14	RES#	Reset signal input. When it's low, initialization of SSD1305 is executed.
15	R/W#	Data write operation is initiated when it's pull low.
16	D/C#	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
17	E/RD#	Data read operation is initiated when it's pull low.
18	NC	No connection
19	DISP	Display off
20	NC	No connection

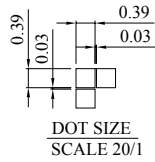
8 0 8 0 INTERFACE.



# 5. Outline Dimension



CON1	
PIN NO.	SYMBOL
1	VDD
2	VSS
3	NC
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	CS
13	NC
14	/RES
15	R/W
16	D/C
17	E
18	NC
19	DISP
20	NC



The non-specified tolerance of dimension is ±0.3mm.

## 6. Optics & Electrical Characteristics

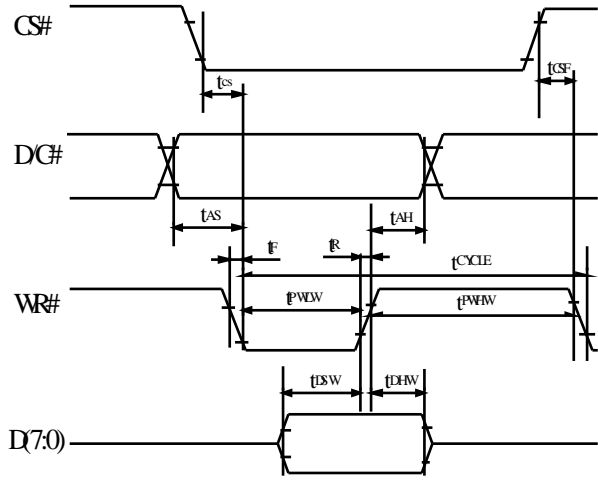
### 6.1 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics  
(VDD-VSS=2.4V to 3.5V, VDDIO=VDD, TA=25°C)

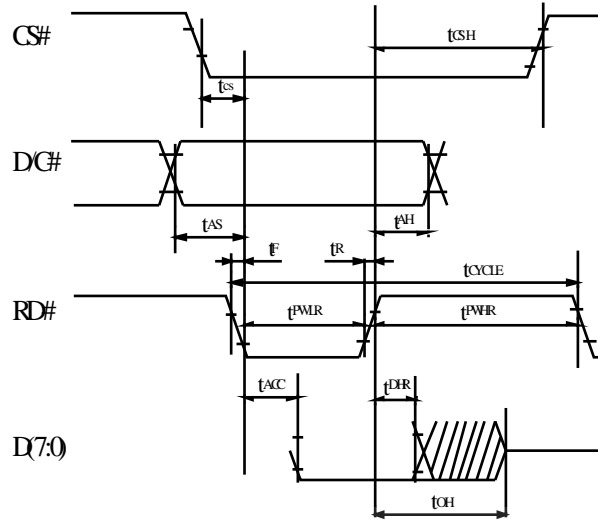
Symbol	Parameter	Min	Typ	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	300	-	-	ns
t <sub>AS</sub>	Address Setup Time	10	-	-	ns
t <sub>AH</sub>	Address Hold Time	0	-	-	ns
t <sub>DSW</sub>	Write Data Setup Time	40	-	-	ns
t <sub>DHW</sub>	Write Data Hold Time	7	-	-	ns
t <sub>DHR</sub>	Read Data Hold Time	20	-	-	ns
t <sub>OH</sub>	Output Disable Time	-	-	70	ns
t <sub>ACC</sub>	Access Time	-	-	140	ns
t <sub>PWLR</sub>	Read Low Time	120	-	-	ns
t <sub>PWLW</sub>	Write Low Time	60	-	-	ns
t <sub>PWHR</sub>	Read High Time	60	-	-	ns
t <sub>PWHW</sub>	Write High Time	60	-	-	ns
t <sub>R</sub>	Rise Time	-	-	15	ns
t <sub>F</sub>	Fall Time	-	-	15	ns
t <sub>CS</sub>	Chip select setup time	0	-	-	ns
t <sub>CSH</sub>	Chip select setup hold time to read signal	0	-	-	ns
t <sub>CSF</sub>	Chip select setup hold time	20	-	-	ns

8080-seriesparallel interface characteristics (Fom 1)

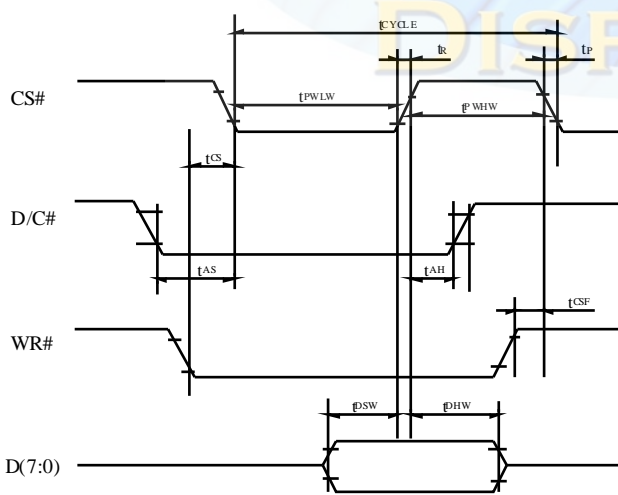
Write cycle(Form1)



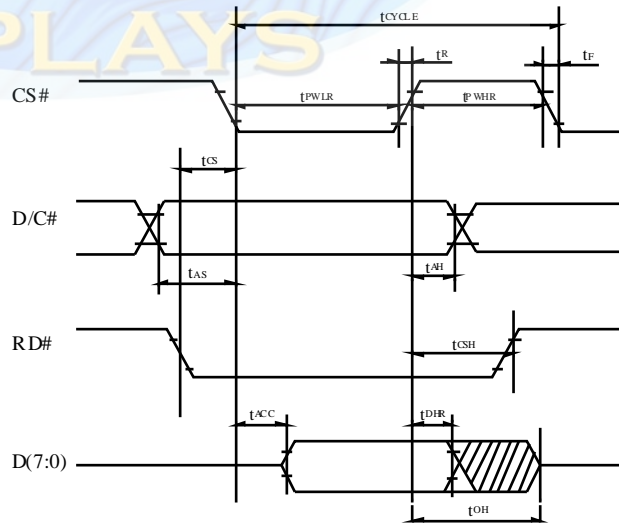
Write cycle(Form1)



Write cycle(Form 2)



Write cycle(Form 2)



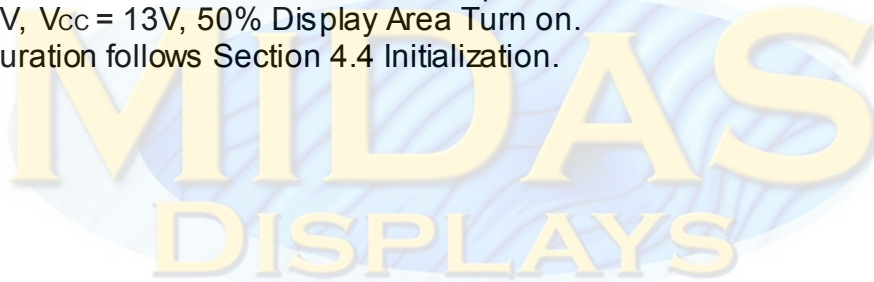
## 6.2 DC Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	2.4	2.7	3.5	V
Supply Voltage for Display	VCC	—	11.0	13.0	15.0	V
High Level Input	VIH	Iout = 100μA, 3.3MHz	0.8×VDD	—	VDD	V
Low Level Input	VIL	Iout = 100μA, 3.3MHz	0	—	0.2×VDD	V
High Level Output	VOH	Iout = 100μA, 3.3MHz	0.9×VDD	—	VDD	V
Low Level Output	VOL	Iout = 100μA, 3.3MHz	0	—	0.1×VDD	V
Operating Current for VDD	IDD	Note 4	—	95	—	mA
Sleep Mode Current for VDD	IDD, SLEEP		—	—	1.5	mA

Note 3: Brightness ( $L_{br}$ ) and Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics and the customer's request.

Note 4:  $V_{DD} = 2.7V$ ,  $V_{CC} = 13V$ , 50% Display Area Turn on.

\* Software configuration follows Section 4.4 Initialization.



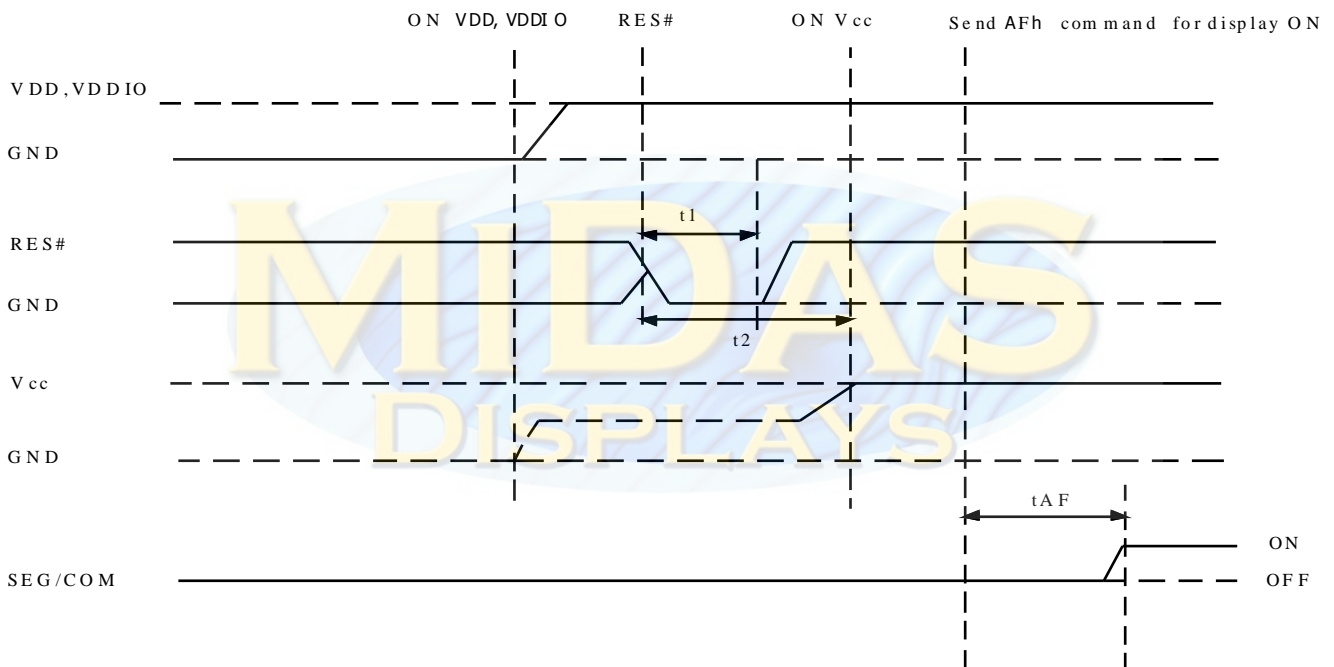
# 7. Block Diagram

## 7.1. POWER ON/OFF SEQUENCE & APPLICATION CIRCUIT

### 7.1.1 POWER ON/OFF SEQUENCE

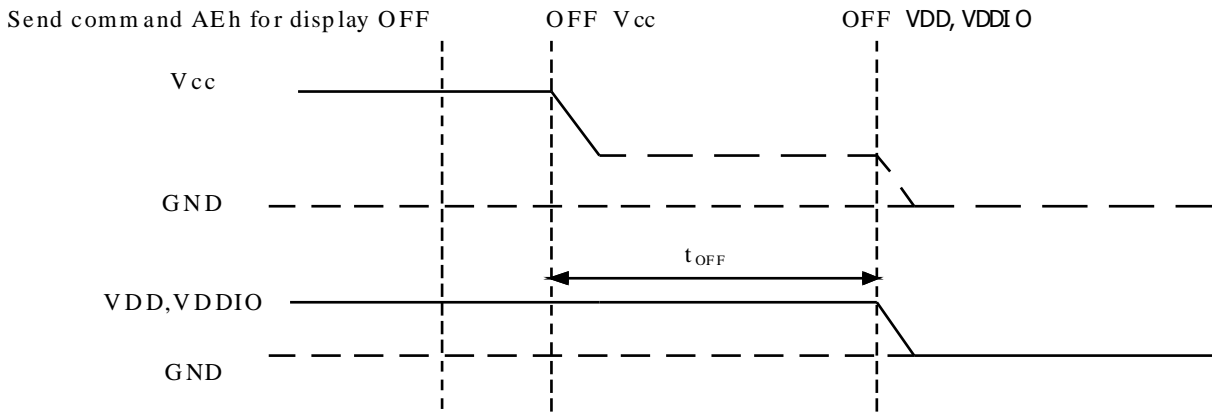
Power ON sequence

1. Power ON VDD ,VDDIO
2. After VDD ,VDDIO become stable , set RES# pin LOW (logic low) for at least 3us( $t_1$ ) and then HIGH (logic high).
3. After set RES# pin LOW (logic low),wait for at least 3us( $t_2$ ). Then Power ON Vcc. (1)
4. After Vcc. become stable , send command AFh for display ON. DEG/COM will be ON after 100ms( $t_{AF}$ ).



### Power OFF sequence

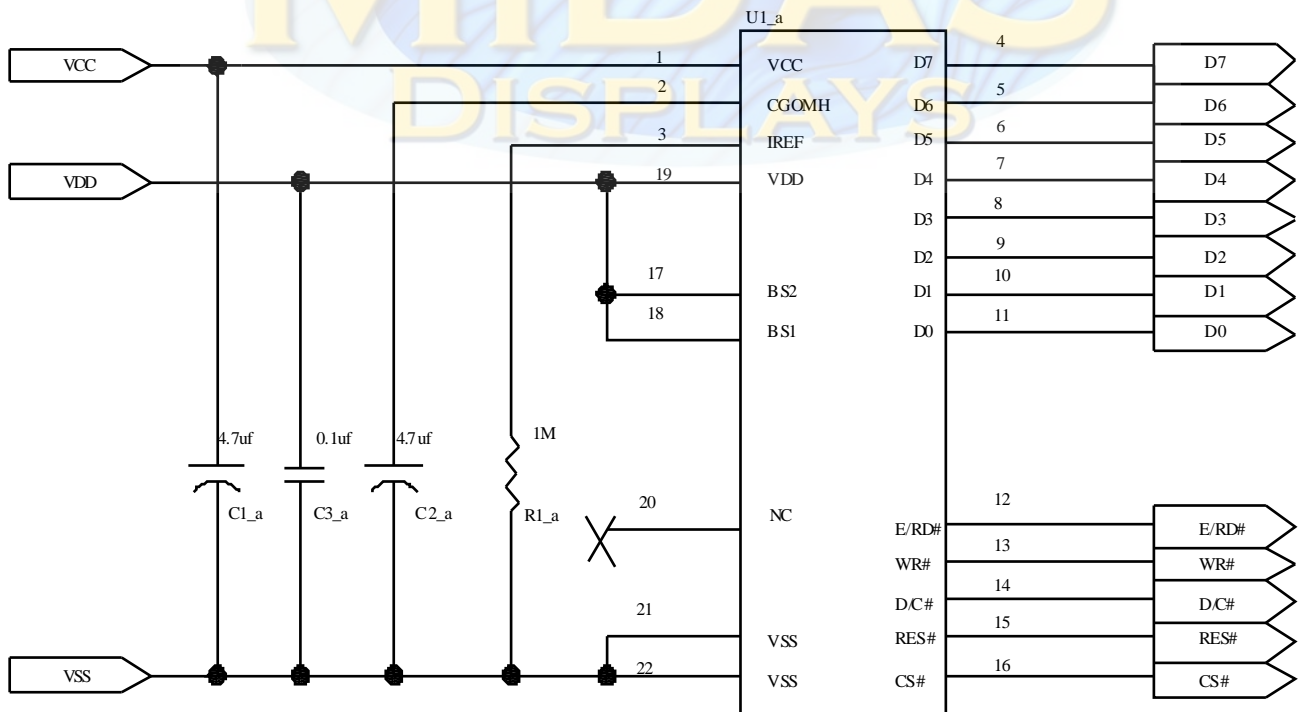
1. Send command AEh for display OFF.
2. Power OFF Vcc.(1),(2)
3. Wait for  $t_{OFF}$ . Power OFF VDD ,VDDIO. (where Minimum  $t_{OFF}$ =80ms,Typical  $t_{OFF}$ =100ms)



**Note:**

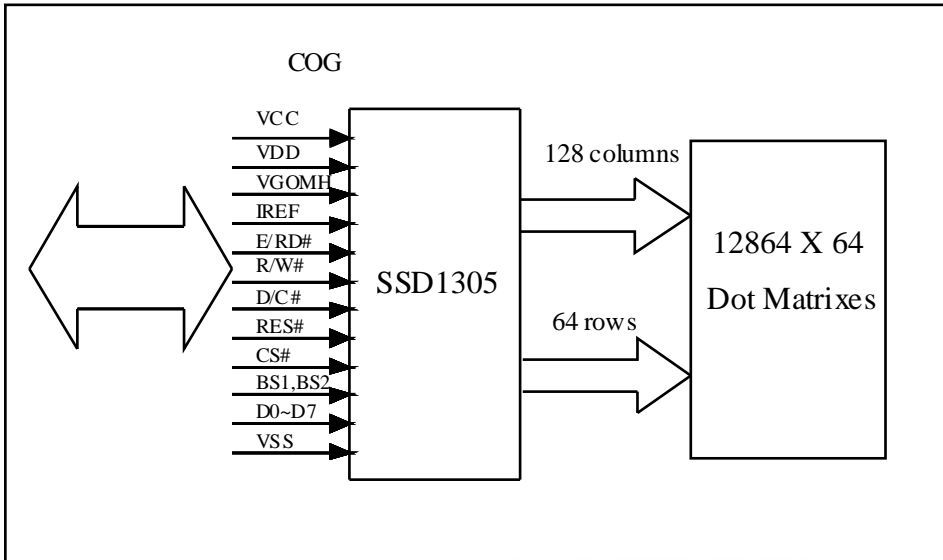
- (1) Since an ESD protection circuit is connected between VDD ,VDDIO and Vcc, Vcc becomes lower than VDD and VDD , VDDIO is ON and Vcc is OFF as shown in the dotted line of Vcc in above figures.
- (2) Vcc should be disabled when it is OFF.

**7.2 APPLICATION CIRCUIT**

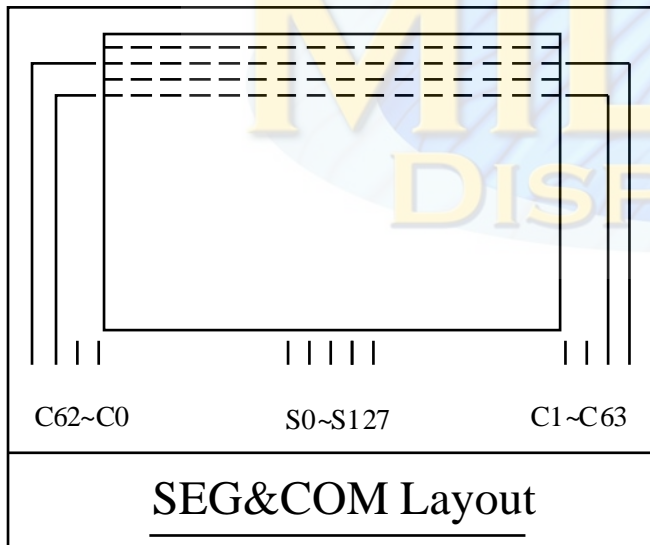


### 7.3 INTERFACE

#### 7.3.1 FUNCTION BLOCK DIAGRAM



#### 7.4 PANEL LAYOUT DIAGRAM





## 8. Reliability

### 8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	80 °C, 240hrs -40 °C, 240hrs	The operational functions work.
High Temperature Storage Low Temperature Storage	80 °C, 240hrs -40 °C, 240hrs	
High Temperature/Humidity Operation/ Thermal Shock	60 °C, 90%RH, 120hrs , -40 °C 80 °C , 24cycles 1 hr dwell	

\* The samples used for the above tests do not include polarizer.

\* No moisture condensation is observed during tests.

### 8.2 Lifetime

Parameter	Min	Typ	Max	Unit	Condition	Notes
Operating Life Time		50,000	—	Hrs	60 cd/m <sup>2</sup> , 50% Checkerboard	6

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

### 8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C; 55±15% RH.

## 9. Absolute Maximum Ratings


Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	3.5	V	1,2
Supply Voltage for Display	VCC	8	16	V	1,2
Operating Temperature	TOP	-40	80	°C	—
Storage Temperature	TSTG	-40	80	°C	—

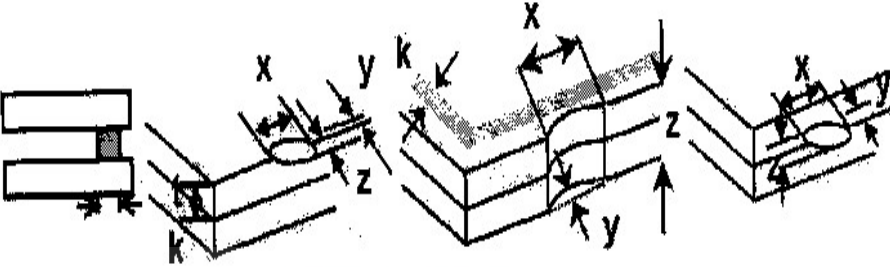
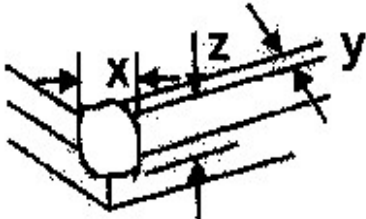
Note 1: All the above voltages are on the basis of "VSS = 0V".

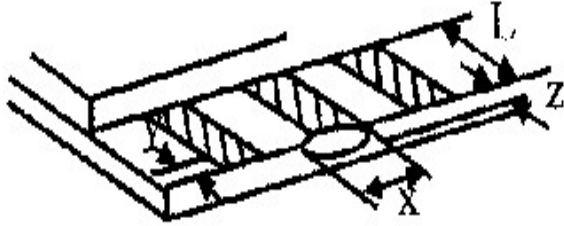

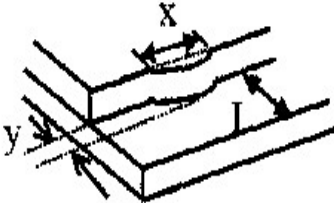
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

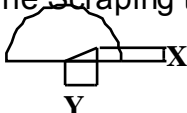


## 10. Inspection specification

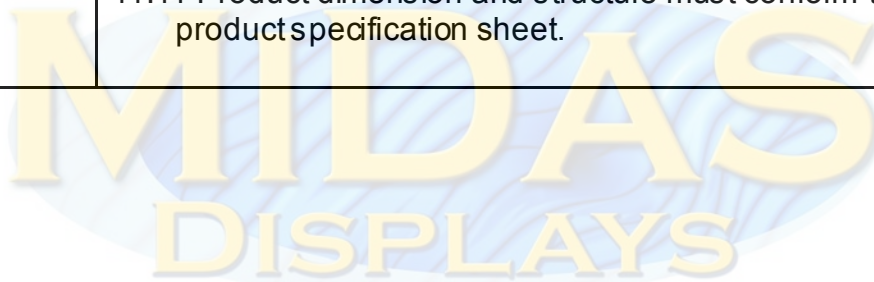
NO	Item	Criterion	AQL												
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 View ing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65												
02	Black or bright spots on OLED (display only)	2.1 Bright and black spots on display $\leq 0.25\text{mm}$ , no more than three Bright or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5												
03	Black spots, bright spots, contamination (non-display)	3.1 Round type : As follow ing draw ing $\Phi = (x + y) / 2$	2.5												
		3.2 Line type : (As follow ing draw ing) <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>W \leq 0.02</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>L \leq 3.0</math></td> <td><math>0.02 &lt; W \leq 0.03</math></td> <td rowspan="2">2</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.03 &lt; W \leq 0.05</math></td> </tr> <tr> <td>---</td> <td><math>0.05 &lt; W</math></td> <td>As round type</td> </tr> </tbody> </table> 		Length	Width	Acceptable QTY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	---
Length	Width	Acceptable QTY													
---	$W \leq 0.02$	Accept no dense													
$L \leq 3.0$	$0.02 < W \leq 0.03$	2													
$L \leq 2.5$	$0.03 < W \leq 0.05$														
---	$0.05 < W$	As round type													
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Size <math>\Phi</math></th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.20</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.50</math></td> <td>3</td> </tr> <tr> <td><math>0.50 &lt; \Phi \leq 1.00</math></td> <td>2</td> </tr> <tr> <td><math>1.00 &lt; \Phi</math></td> <td>0</td> </tr> <tr> <td>Total QTY</td> <td>3</td> </tr> </tbody> </table>	Size $\Phi$	Acceptable QTY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total QTY	3	2.5
Size $\Phi$	Acceptable QTY														
$\Phi \leq 0.20$	Accept no dense														
$0.20 < \Phi \leq 0.50$	3														
$0.50 < \Phi \leq 1.00$	2														
$1.00 < \Phi$	0														
Total QTY	3														

NO	Item	Criterion	AQL																		
05	Scratches	Follow NO.3 black spots, bright spots, contamination																			
06	Chipped glass	<p>Symbols Define:  x: Chip length      y: Chip width      z: Chip thickness  k: Seal width      t: Glass thickness      a: OLED side length  L: Electrode pad length:</p> <p>6.1 General glass chip :  6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="437 987 1177 1207"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td><math>Z \leq 1/2t</math></td> <td>Not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> <tr> <td><math>1/2t &lt; z \leq 2t</math></td> <td>Not exceed 1/3k</td> <td><math>x \leq 1/8a</math></td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p>  <table border="1" data-bbox="437 1547 1177 1767"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td><math>Z \leq 1/2t</math></td> <td>Not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> <tr> <td><math>1/2t &lt; z \leq 2t</math></td> <td>Not exceed 1/3k</td> <td><math>x \leq 1/8a</math></td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is the total length of each chip.</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			
z: Chip thickness	y: Chip width	x: Chip length																			
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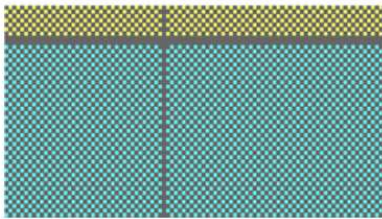
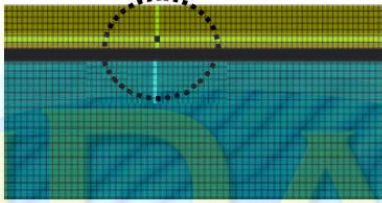

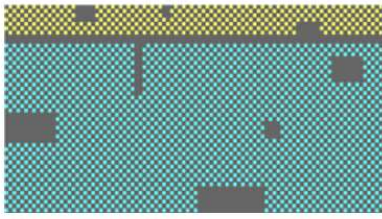
NO	Item	Criterion	AQL								
06	Glass crack	<p>Symbols :</p> <p>x: Chip length      y: Chip width      z: Chip thickness  k: Seal width      t: Glass thickness      a: OLED side length  L: Electrode pad length</p> <p>6.2 Protrusion over terminal :</p> <p>6.2.1 Chip on electrode pad :</p>  <table border="1" data-bbox="443 842 1118 958"> <thead> <tr> <th>y: Chip width</th> <th>x: Chip length</th> <th>z: Chip thickness</th> </tr> </thead> <tbody> <tr> <td><math>y \leq 0.5\text{mm}</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </tbody> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$			
		y: Chip width	x: Chip length	z: Chip thickness							
$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$									
<p>6.2.2 Non-conductive portion:</p>  <table border="1" data-bbox="496 1285 1115 1402"> <thead> <tr> <th>y: Chip width</th> <th>x: Chip length</th> <th>z: Chip thickness</th> </tr> </thead> <tbody> <tr> <td><math>y \leq L</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </tbody> </table> <p>⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙ If the product will be heat sealed by the customer, the alignment mark not be damaged.</p> <p>6.2.3 Substrate protuberance and internal crack.</p>  <table border="1" data-bbox="850 1641 1227 1720"> <thead> <tr> <th>y: width</th> <th>x: length</th> </tr> </thead> <tbody> <tr> <td><math>y \leq 1/3L</math></td> <td><math>x \leq a</math></td> </tr> </tbody> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$x \leq a$	2.5
y: Chip width	x: Chip length	z: Chip thickness									
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$									
y: width	x: length										
$y \leq 1/3L$	$x \leq a$										

NO	Item	Criterion	AQL
07	Cracked glass	The OLED with extensive crack is not acceptable.	2.5
08	Bezel	8.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 8.2 Bezel must comply with job specifications.	2.5 0.65
9	PCB , COB	9.1 COB seal may not have pinholes larger than 0.2mm or contamination. 9.2 COB seal surface may not have pinholes through to the IC. 9.3 The height of the COB should not exceed the height indicated in the assembly diagram. 9.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 9.5 No oxidation or contamination PCB terminals. 9.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 9.7 The jumper on the PCB should conform to the product characteristic chart. 9.8 If solder gets on bezel tab pads, zebra pad or screw hold pad, make sure it is smoothed down. 9.9 The Scraping testing standard for Copper Coating of PCB <div style="text-align: center; margin-top: 10px;">  <p data-bbox="742 1444 949 1489"><math>X * Y \leq 2\text{mm}^2</math></p> </div>	2.5 2.5 0.65 2.5 0.65 0.65 2.5 2.5
10	Soldering	10.1 No un-melted solder paste may be present on the PCB. 10.2 No cold solder joints, missing solder connections, oxidation or icide. 10.3 No residue or solder balls on PCB. 10.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
11	General appearance	11.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		11.2 No cracks on interface pin (OLB) of TCP.	0.65
		11.3 No contamination, solder residue or solder balls on product.	2.5
		11.4 The IC on the TCP may not be damaged, circuits.	2.5
		11.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it causes the interface pin to sever.	2.5
		11.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	2.5
		11.7 Sealant on top of the ITO circuit has not hardened.	0.65
		11.8 Pin type must match type in specification sheet.	0.65
		11.9 OLED pin loose or missing pins.	0.65
		11.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		11.11 Product dimension and structure must conform to product specification sheet.	0.65



### Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	